An On-Chip Spectrum Analyzer for Signal Integrity Estimation of High Speed Serial Links

Jeonghyeon Cho[1], Woojin Lee [2], Eakhwan Song [3], Jongjoo Shim[4],
Minchul Shin[5], Changwook Yoon[6], Joungho Kim [7]

Terahertz Interconnection and Package Laboratory, Department of Electrical Engineering,
Korea Advanced Institute of Science and Technology (KAIST),
373-1 Guseong-dong, Yuseong-gu, Daejeon, Korea
[1]caleb1@ eeinfo.kaist.ac.kr
[7]joungho@ee.kaist.ac.kr

***Abstract*— We present an on-chip spectrum analyzer (OSA) to estimate signal integrity of high speed serial links. The proposed OSA is composed of an on-chip sine-wave generator (OSG) and an on-chip amplitude detector (OAD), which are physically implemented in a four-metal, 1.8 V, 0.18 um standard CMOS technology. The implemented OSA is experimentally verified with a characterization of High-Definition Multimedia Interface (HDMI) cables, which confirmed that the implemented OSA can successfully provide transfer functions of the channels up-to 1.5 GHz. Finally, this paper also investigates the good potentiality of the proposed OSA for high speed equalizer applications.**

Key words: Spectrum analyzer, equalizer, sine-wave generator, amplitude detector, high speed data transmission, high speed channel, transfer function.

I. INTRODUCTION

For a higher speed of data transmission, research on channels and circuits for high speed operations is required. Recently, the revolutionary progress in CMOS technology has enabled the implementation of several tens of Gbps circuits [1]. However, for channels, the physical limitations of transmission media complicate their over Gbps application and impose considerable expenses on even the most minute of improvements.

Non-ideal channel effects--such as conductor and dielectric loss, reflection, and crosstalk--make high speed data transmission difficult [2]. Among these effects, reflection and crosstalk may be overcome with careful design considerations, while the losses are intrinsic phenomena. Moreover, the losses increase with frequency and result in Inter Symbol Interference (ISI). Hence, conductor and dielectric loss will be main obstacles to the 10 Gbps regime.

Equalizers are the most widely used circuit elements to overcome channel loss. In principal, an equalizing is to artificially manipulate the transfer characteristics of the transmitter (or receiver) reciprocal to a channel. Accordingly, a fundamental requirement is to recognize the transfer characteristics of a channel, and there are many kinds of equalizers that provide this function [2].

Existing equalizers estimate the transfer function of a channel with indirect methods since: (1) the transfer function does not reflect real time channel characteristics; and (2) there are rarely on-chip schemes that can estimate the channel transfer function. For reason (1), in real world applications a channel does not change as much with time as its application. In other words, in most cases, a channel can be regarded as a time invariant component. Hence, occasional measurements at start-up or at various time intervals can sufficiently reflect the long-term characteristics of channel. For reason (2), there has been some movement to use on-chip spectrum analyzers (OSAs) as enablers [3], but the performance requirement for this application is a bit excessive. To apply them to equalizer application, they must be equipped with a wide bandwidth signal generator and an amplitude detector, which is still challenging.

In this paper, we introduce an on-chip spectrum analyzer (OSA) scheme that is suitable for high speed equalizer applications. It utilizes only simple conventional circuit elements to guarantee low cost, low power, and high frequency feasibility. It is physically implemented in silicon and validated to apply them to estimate the transfer functions of commercial High-Definition Multimedia Interface (HDMI) cables. The proposed OSA scheme successfully provides a direct measurement method for high speed data transmission channels.

II. ON-CHIP SPECTRUM ANALYZER (OSA) ARCHITECTURE

The block diagram of the proposed OSA is shown in Fig. 1. The OSA is composed of an on-chip sine-wave generator (OSG), an on-chip amplitude detector (OAD), and a channel under test (CUT). The function of the OSG and the OAD mimics that of a commercial spectrum analyzer (SA). That is, the OSG generates a series of single tone signals with constant amplitude, transmits them through a CUT, and the OAD measures the amplitude of the transferred data at the receiver side.

The transfer function of a CUT is obtained in the same fashion as a SA. That is, the function is extracted by dividing the amplitude of the received signal by that of the transmitted signal, where the amplitude of the transmitted signal is measured by loop-backing a copied OSG signal at the receiver side. The amplitude of the received signal is also obtained by

interconnecting OSG and OAD as close as the DC loss of their interconnection can be ignored.

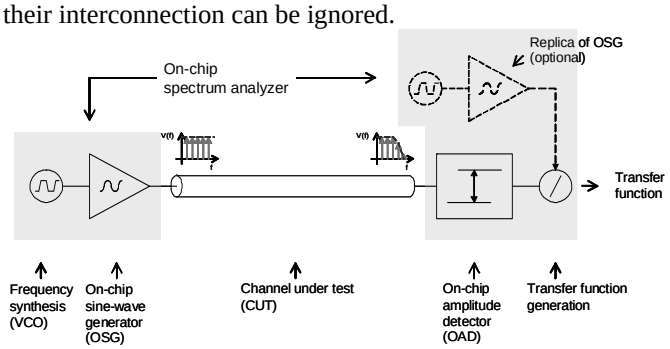


Fig. 1 Block diagram of the proposed OSA.

III. Building Blocks and Circuit Implementation

A. On-chip Sine-Wave Generator (OSG)

A conventional OSG is implemented using an analog oscillator with a filtering section and a non-linear feedback function, where the former removes unwanted harmonics from its output and the latter forces the continuation of oscillation [4]. A OSG can be implemented using a wave shaping method, where signal processing elements such as a digital-to-analog converter or a variable gain step-wise switched-capacitor amplifier reshapes the generated signals into more sine-like waveforms [3]. In this scheme, a filtering section is optional. It is merely used for filtering out unwanted harmonics of generated sine-like signals. Hence, if a wave shaper can generate almost sine-wave-like signals, it can be excluded, which can alleviate the frequency limitation of system -- this is the key idea of the proposed OSG.

Fig. 2 shows the block diagram and the main circuits of the proposed OSG. The main body is composed of a 4-staged voltage controlled ring oscillator (VCO) and a harmonic rejection mixer (HRM) [5]. The VCO has a 4-staged configuration for octal-phase signal generation, and the delay cell of each stage is composed of a symmetric linear load delay cell [6], utilizing its wide tuning range and its other outstanding properties. The HRM is included for rejecting higher order harmonics from square-waves generated by the VCO. The HRM is a kind of wave shaper, in other words, the HRM remakes signals with much smaller high-order harmonics to present almost pure sine-waves without filter circuits. In addition, the HRM is implemented by a simple analog mixer, which more reduces the limitation for high frequency operation of OSG.

B. On-chip Amplitude Detector (OAD)

An analog-to-digital converter (ADC) can be used as an amplitude detector. However, for high speed (or quickly varying) signals, the performance requirement of the ADC is too challenging. Therefore, in this research, the input signal is rectified (or multiplied) and regulated first; then it is used for the input of slow, but high resolution ADC.

Fig. 3 shows the block diagram and the main circuitry of the proposed OAD. The main body is composed of a pair of rectifiers, a pair of operational transconductance amplifiers (OTAs), and a dual-slope ADC. A current mode rectifier is adopted for high speed rectifying operation, where the input signals of rectifiers are delivered in ac-coupled manner to maintain a constant bias point for the input diodes. OTAs play a role in converting the extracted DC voltage components of input signals into the corresponding DC currents and regulating them more. For this purpose, the OTA is designed with adaptive source degeneration [7], followed by a folded cascade stage, which provides constant trans-conductance for wide input dynamic ranges. The DC and V-I conversion makes the requirements of ADC very light. The ADC's inputs are already regulated DC currents. Hence, the speed of the ADC is no longer important. A dual-slope ADC with a simple OTA-C integrator is used in this scheme, which enables more area reduction compared with a conventional one with an operational amplifier (OPA)-C integrator.

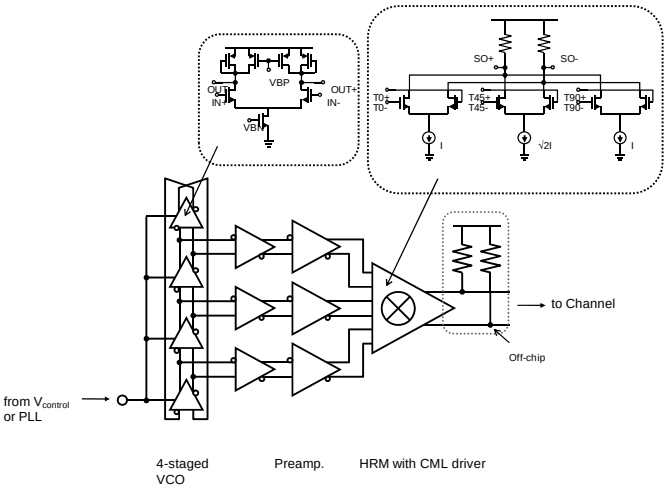


Fig. 2 Block diagram of the implemented OSG and its main circuit elements.

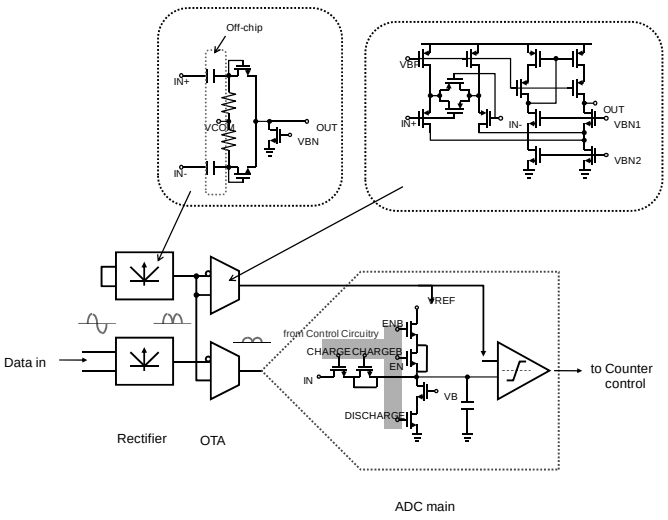


Fig. 3 Block diagram of the implemented OAD and its main circuit elements.

IV. Experimental Results

A. Test Chips

The proposed OSG and OAD are fabricated on two separate test chips for test convenience as shown in Fig.'s 4 and 5. The OSG is fabricated using a four-metal, 1.8 V, 0.18 um standard CMOS technology, with an oscillation frequency from below 10 MHz up to 1.5GHz. It occupies an active area of 300 um x 200 um and consumes a maximum power of 70 mW. The OAD is fabricated by using the same silicon process, with operating frequencies over 1GHz. (If there was not a stability issue, the operating frequency may extend up to over 2.5GHz.) It occupies an active area of 450 um x 300 um and consumes a maximum power of 70mW.

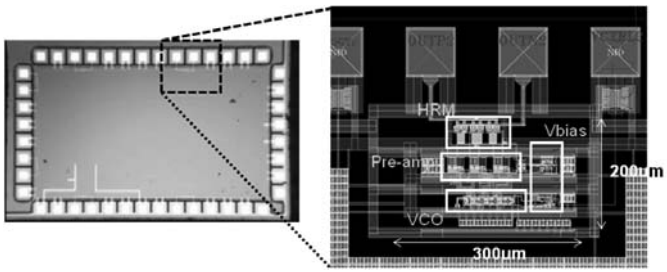


Fig. 4 Photomicrograph of the fabricated OSG and its layout view.

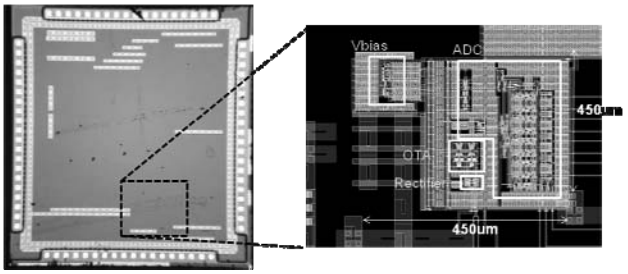


Fig. 5 Photomicrograph of the fabricated OAD and its layout view.

B. Characterization of the fabricated OSG and OAD

Fig. 6 shows the FFT results obtained from the fabricated OSG and an on-chip square-wave generator (OSQG). The first test chip also has an OSQG for validating the implemented OSG via comparison. The OSQG is comprised of the same type of VCO and a HRM with single-phase inputs. The FFT results are normalized to their fundamental frequency values to compare their harmonic rejection properties. As shown in the graphs, at high frequencies, both of the waveform generators demonstrate good harmonic rejection properties, which is due to the low pass filter (LPF) characteristics of the engaged circuits. However, as frequencies go down, the harmonic rejection noticeably differs and the capability of the OSG is superior to that of the OSQG. That is, the OSG can provide almost pure sine-wave signals with wide frequency range, which is a principal element for OSA.

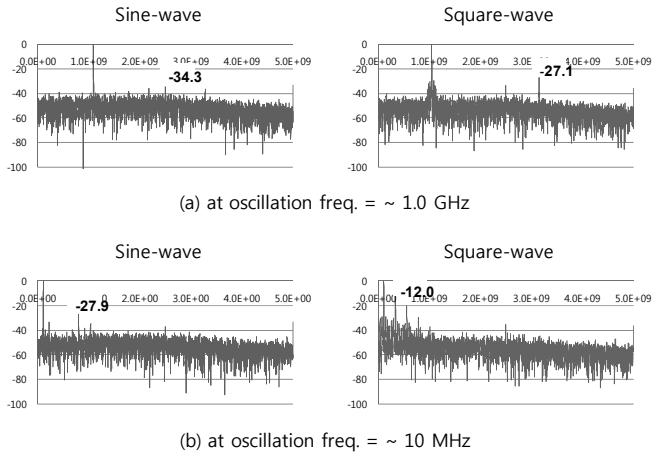


Fig. 6 FFT results for the generated sine/square waves

Fig. 7 shows the measured digital output value versus input signal levels in the fabricated OAD. As shown in the graph, for a wide range of input levels, the linearity of the OAD is maintained. In reality, the detection levels of a rectifier are proportional to the square of the input levels. However, for high input levels, the nonlinearity of the OTA degrades the slope of this graph. Consequently, the overall slope of the detected levels vs. input signal levels looks linear on the whole.

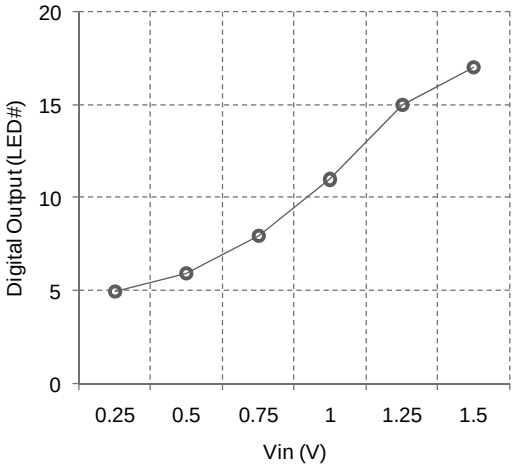


Fig. 7 Measured digital output data versus input signal levels in the fabricated OAD.

C. Validation of the Proposed OSA

Fig. 8 shows a test set-up for verifying the proposed OSA scheme, where a OSG chip directly mounted on a test board plays the role of a variable single tone signal generator, the OAD chip--assembled in the same manner--measures the levels of received signals, and two HDMI cables from Molex Inc. with different lengths are used for CUTs.

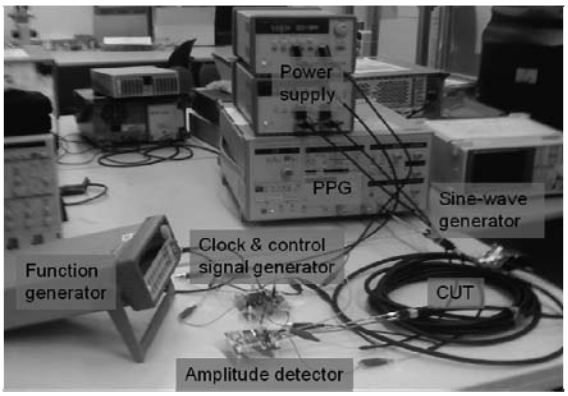


Fig. 8 Measurement set up to verify the implemented OSA.

The measured results for engaged CUTs are displayed in Fig. 9. The characteristics of channels are easily analyzed by a commercial vector network analyzer (VNA). Therefore, the results obtained by the proposed OSA are compared with those from N5230A, a VNA from Agilent technologies. In the graph, straight lines are the results from N5230A, while the dotted symbols are the results from the implemented OSA. As shown in the graph, the implemented OSA extracts the transfer function of CUTs quite well.

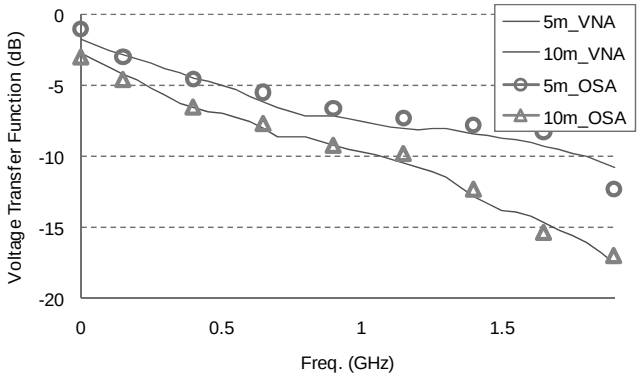
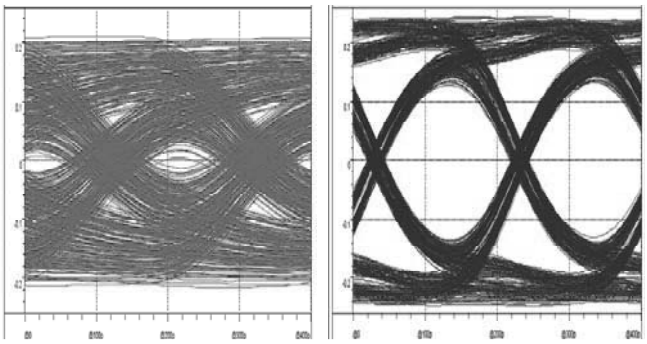


Fig. 9 Measured transfer characteristics of HDMI cables. (a) by a commercial VNA (straight lines), and (b) by the implemented OSA (dotted symbols) after numerical correction.

D. Investigation of the Proposed OSA for High Speed Equalizer Applications

This paragraph briefly investigates the possibility of the proposed OSA for high speed equalizer applications.

Fig. 10 (a) shows the eye diagram obtained by HSPICE channel simulation for a 5 m long HDMI cable with 5 Gbps PRBS data. As it can be seen, the eye opening is almost closed by the excessive high frequency loss of the channel, which is estimated to about 9 dB at 1.5 GHz by N5230A. In the similar manner, the proposed OSA provides pertinent data to the losses of a channel with frequencies. Hence, these data can be used for channel equalization. Fig. 10 (b) shows the eye diagram for the equalized waveform, where the equalizing information is extracted by the proposed OSA and the data only at 100 MHz and 1.5 GHz are used. As it can be expected, the eye is widely opened even at 5 m long, 5 Gbps data rate.



(a) w/o equalization (b) w/ equalization

Fig. 10 HSPICE simulation results for a 5 m long HDMI cable at 5 Gbps data rate. (a) without equalization, (b) with equalization

V. CONCLUSION

We have introduced an OSA scheme suitable for characterizing high speed data channels. For this purpose, the two main building blocks--an OSG and an OAD--are designed and implemented using a four-metal, 1.8 V, 0.18 um, standard CMOS technology, showing their capability for Gbps applications. The designed OSA is then applied to validate the proposed OSA scheme. The measurement results show that the proposed OSA scheme is viable for high speed equalizer applications.

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