A Study on Prediction of Parallel Impedance of Closely Mounted Bypass Capacitors

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***Abstract*— In this paper, the effective layout of decoupling capacitors to minimize the IC power supply impedance is discussed. A simple model to estimate the mutual inductance between two bypass capacitors is proposed. By using this model, an easy, more accurate impedance prediction of the parallel, closely mounted capacitors become possible. The impedance when the capacitors were used in several typical layouts was calculated by this method. The results ware verified by the measurement. Also, effective layout to decrease impedance is discussed. This technique is applied to 3-terminal capacitor.**
Key words: decoupling, bypass, capacitor, PDN, PDS, impedance.

I. INTRODUCTION

As a high-speed digital IC, to minimize the power supply impedance is one of the impotant issue to control voltage fluctuations and to prevent an electromagnetic noise. In general, bypass capacitor is used to decrease impedance of power supply circuit. However, in the high frequency, to control power supply impedance small becomes very difficult by the action of parasitic inductance (ESL) of the capacitor. To decrease influence of ESL, many capacitors are connected parallel with the power supply terminal as shown in Fig. 1, to minimize impedance by a parallel effect.

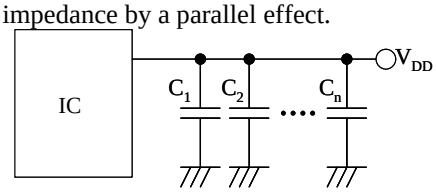


Fig. 1. Bypass capacitors connected to IC power supply.

When the capacitor is used in parallel as Fig. 2, and arranged in overcrowded layout as shown in Fig.2 (a), there is a possibility that ESL grows by the influence of mutual inductance M between capacitors, and the impedance-decreasing effect becomes small. To avoid this influence, if the capacitor is arranged apart, like Fig. 2 (b), mutual inductance M should become small. But in this layout, the distance between power terminal and capacitors should increase, and it might cause another impedance. Therefore, to minimize the power supply impedance, deciding an appropriate interval of the capacitor becomes important issue.

On the other hand, if the mutual inductance M between capacitors is positively used, there might be a possibility that ESL can be reduced in equivalence. This layout technique has been already mentioned in some documents (e.g., [1]).

Usually, 3D electromagnetic field simulator is useful to predict such layout effect, which include capacitor's mutual inductance. However, it needs huge calculation resource. Then, it is useful to examine the layout effect if there is a simple technique that can understand a rough tendency.

In this paper, to make the problem simple, the case where only two capacitors were used was assumed. The capacitor was modeled as a thin wire, and the mutual inductance between these wires was calculated in the electromagnetism, and it was used to calculate the impedance of the parallel-capacitor circuit.

By using this method, the impedance when the capacitors was arranged at opposite position, or arranged at side-by-side position was calculated. The results were verified by measurement.

II. CALCULATION OF MUTUAL INDUCTANCE

Fig. 3 (a) shows a simple model that two bypass capacitors (C_1, C_2) are installed on the IC power supply circuit. Considering ESL of the capacitor, this circuit can be shown like Fig. 3 (b). Here, the mutual inductance M_{12} changes according to the relative position of the capacitors.

Fig. 4 shows three typical layouts of the capacitor. Layout A (side-by-side) shows the case in where capacitors are placed at the same side in parallel with distance *d*. And layout B (opposite side) shows another case in where capacitors are placed at the opposite side with distance *d* and *δ*.

Also, layout C is possible. There, C_2 is squarely arranged for C_1. But in this case, mutual inductance should not be generated. Therefore, layout C is excluded in this paper.

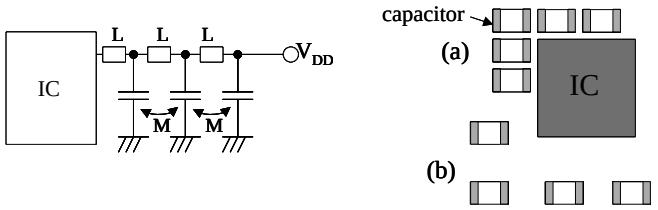


Fig. 2. Examples of capacitor placement.

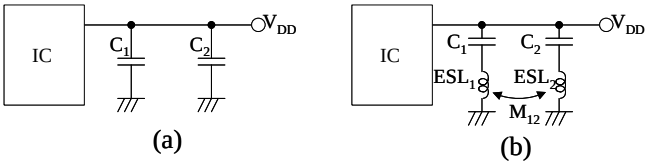


Fig. 3. Equivalent circuits of parallel bypass capacitors.

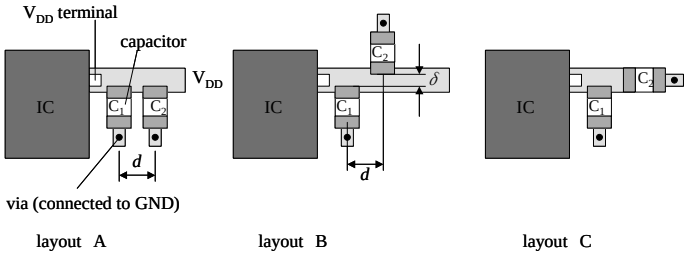


Fig. 4. Typical layouts of bypass capacitors.

In general, the inductance between two wire elements is described as a partial inductance. This partial inductance can be obtained by integrating the magnetic vector potential (formed with the current that flows on another wire) on the wire, and dividing this integrated result by the current [2].

Therefore, the mutual inductance M_{12} is shown by the following expressions [3]. There, the capacitor is modeled as a thin wire, and assumed to be able to disregard width and the thickness. And capacitors layout is assumed to be parallel to x-axis as shown in Fig. 5.

$$M_{12} = \frac{\mu_0}{4\pi}\int_{a_2}^{b_2}\int_{a_1}^{b_1}\frac{1}{r_{12}}dx_1dx_2 \qquad (1)$$

Here μ_0 is the permeability of a vacuum.

And r_{12} is the distance between wire elements shown as follows.

$$r_{12} = \sqrt{d^2 + (x_1 - x_2)^2} \qquad (2)$$

Also, l_1 and l_2 are the length of capacitor body, d and δ show the distance between capacitors.

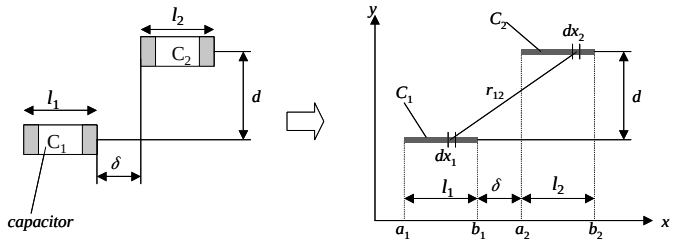


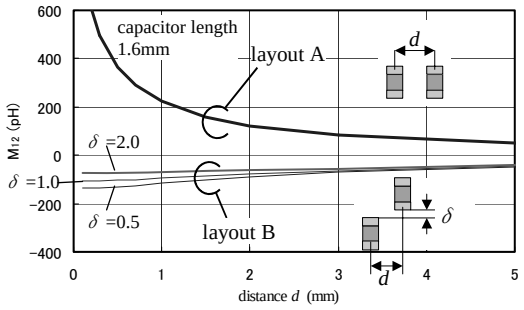
Fig. 5. Wire model of two parallel capacitors.

Fig. 6 shows the example of calculated M_{12}. Here, (a) 1.6 × 0.8 mm size or (b) 3.2 × 1.6 mm size monolithic ceramic capacitor (MLCC) is assumed. The wire length l_1 and l_2 are adjusted to 1.6mm or 3.2 mm respectively. In equation (1), $a_1 = a_2$, $b_1 = b_2$, $a_1 + l_1 = b_1$ for layout A. And also, $a_1 + l_1 = b_1$, $a_2 + l_2 = b_2$, $a_2 = a_1 + l_1 + \delta$ for layout B.

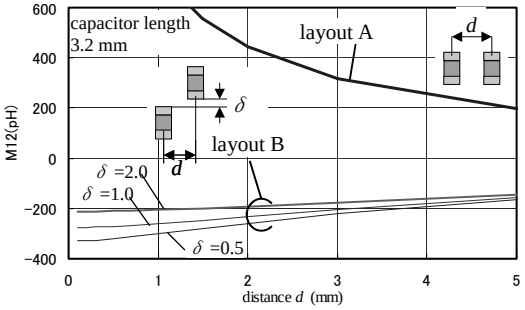
Consideration of the direction of the current, the sign of M_{12} is applied to the plus for Layout A, and to the minus for layout B.

In general, the typical self-inductance value of the 1.6 × 0.8 mm size MLCC capacitor is from 0.5 to 1nH. The result of Fig. 6 shows that the mutual inductance is not able to disregard for the self-inductance when distance d between capacitors is 1 or 2 mm or less.

Moreover, the results show the tendency that layout A (side-by-side) increases ESL while layout B (opposite side) decreases it.



(a)



(b)

Fig. 6. Calculated mutual inductance. (a) 1.6 mm length capacitor. (b) 3.2 mm length capacitor.

III. Experimental Confirmation

The calculation method that had been explained in Chapter 2 was verified as follows by the measurement of the impedance of the parallel capacitors.

Fig. 7 shows the measured sample. The impedance on the micro-strip line (MSL) where the capacitor was installed in was measured. This MSL assumed the power supply line shown in Fig. 4. And the measured results were compared with the calculated impedance by using the mutual inductance described in Chapter 2.

Here, two MLCC with same nominal capacitance of 0.01 μF in 1.6 × 0.8 mm size were installed in the layout that corresponds to layout A (side-by-side), or layout B (opposite side).

The impedance was converted from S_{11} measured with the vector network analyzer (VNA) connected through the SMA connector. The electric length was corrected to determinate impedance in the point to capacitor C_1 have installed

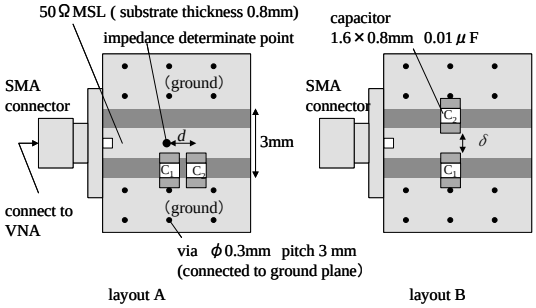


Fig. 7. Measurement sample.

A. Determination of Capacitor Parameters

At the first, the impedance when capacitor C_1 was installed alone was measured, and the equivalent circuit parameter of C_1 and C_2 was provided based on this measured value. The result of providing was Cap. = 0.01μF, ESL = 0.53 nH, ESR = 0.025 ohm (series CLR circuit). This value was provided from low-frequency impedance and the self-resonant frequency.

From this equivalent circuit parameter, the impedance when the two capacitors simply tied parallel was calculated. Fig. 8 shows the result. Here, impedance for single capacitor and two parallel capacitors are indicated. Measured results are also plotted for comparison. For the case of two capacitors, layout A is used.

When single capacitor is used, the calculated result and the measured result are corresponding. On the other hand, when two capacitors are used, the self-resonant frequency is different, and a big difference is seen in the frequency of 70MHz or more. The reason of this difference, as mentioned in Chapter 1, is thought that the mutual inductance between capacitors affected.

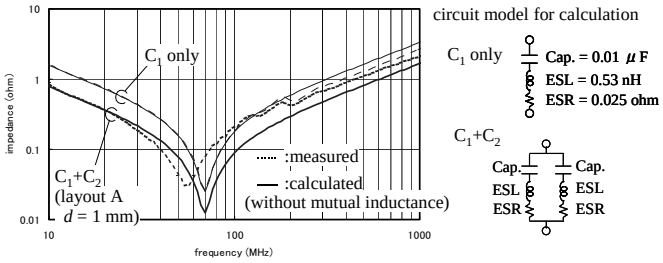


Fig. 8. Calculated result without mutual inductance.

B. Calculation of Mutual Inductance

For the next step, the mutual inductance M_{12} at layout A (side-by-side), and layout B (opposite side) was calculated by using equation (1). Here, parameters ware set based on the experiment circuit shown in Fig. 7. As for the result of M_{12}, layout A where d = 1 mm became 0.222nH, and -0.096nH at layout B where d = 0 mm and δ = 1 mm.

Fig. 9 shows the calculated result when these values were reflected in the equivalent circuit model. As for layout A (side-by-side), the influence of 1mm MSL between two capacitors was considered. There, Z_0 means the characteristic impedance, and β is phase constant, and l (= d) is the length between capacitors.

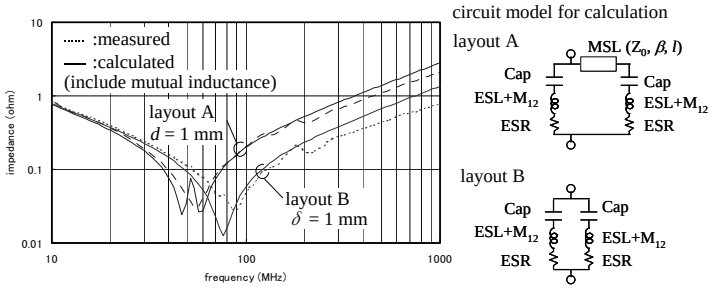


Fig. 9. Calculated result includes mutual inductance.

C. Comparison Between Calculated Result and Measured Result

Fig. 9 also shows the measured result for comparing with the calculated value. These show good agreement in the frequency of 200MHz or less. From these results, it is confirmed that the calculation method in Chapter 2 is effective.

Moreover, it is thought that layout B (opposite side) has more advantageous than layout A (side-by-side) to decrease impedance. The difference might become twice or more by the frequency of 100MHz or more.

IV. CONSIDERATION

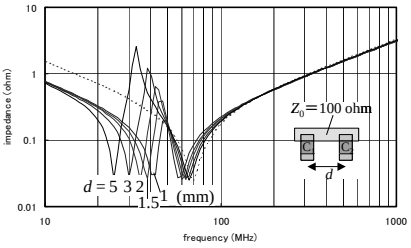
A. Influence of the Distance Between Side-by-side Capacitors

The reason why layout B had more advantageous than layout A to decrease impedance is thought that the sign of the mutual inductance is different. In layout A, mutual inductance is added to original ESL in the direction of plus. Therefor, reduction of mutual inductance is important.

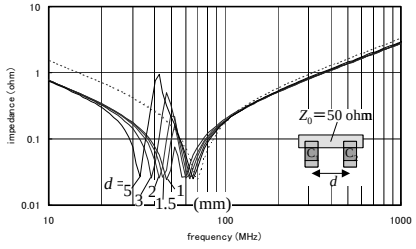
To decrease the mutual inductance in layout A, we can increase the distance between capacitors. However, it is necessary to think about an increase of the line inductance between capacitors.

Then, the impedance when distance d between capacitors was changed was examined. Fig. 10 shows the result. Here, Z_0 indicate the characteristic impedance of line between capacitors. Solid line shows the calculated result when two capacitors are used, while doted line shows the calculated result when only C_1 capacitor is used for the comparison.

Fig. 10 shows the tendency that there is little controlling effect of impedance in the high frequency of 100MHz or more if the capacitor is used on high Z_0 line. And Fig. 10 also shows the tendency that low Z_0 line is effective to lower the impedance and to decrease the influence of counter resonance at the frequency of 30 to 70 MHz.



(a)



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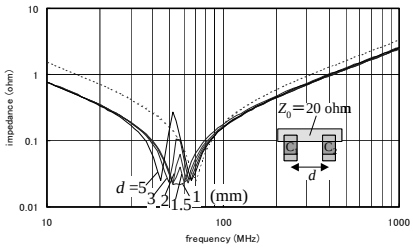
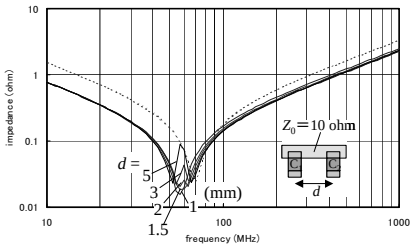


(c)



(d)

Fig. 10. Calculated result in layout A where *d* changed. (a) Z_0 = 100 ohm. (b) Z_0 = 50 ohm. (c) Z_0 = 20 ohm. (d) Z_0 = 10 ohm

Fig. 11 shows another calculated result where Z_0 are changed in the same distance d = 3 mm. We can also find the tendency that the low Z_0 line between capacitors is useful to decrease impedance. However, even if capacitors are used in the extremely low Z_0 line, such as 5 ohm, the impedance doesn't reach the result when capacitors are used in layout B.

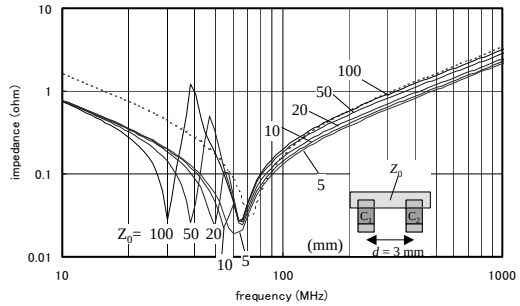


Fig. 11. Calculated results in layout A where Z_0 changed

B. Comparison with 3- Terminal Capacitor

To achieve layout B effect with single component, the 3-terminal capacitor seems to be a good solution, because the ground electrode of 3-terminal capacitor is in the right and left side of parts, so the bypass current will automatically flow in the direction of layout B (see Fig. 12). Originally, the 3-terminal capacitor is effective for the noise reduction with its feed-thru structure; it is thought from above viewpoint that it is also effective to minimize the impedance.

Then, the impedance when 3-terminal capacitor was used was measured and it compared with layout B. Fig. 13 shows the result. Here, 3.2×1.6mm sizes 3-terminal capacitor is used on the same substrate of Fig. 7. From the result of Fig. 13, it is confirmed that the 3-terminal capacitor show low impedance equal with two capacitors used in layout B.

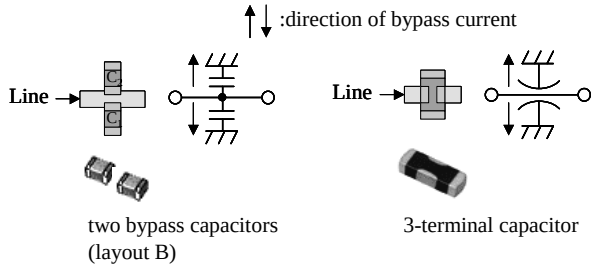


Fig. 12. Circuit construction of the 3-terminal capacitor.

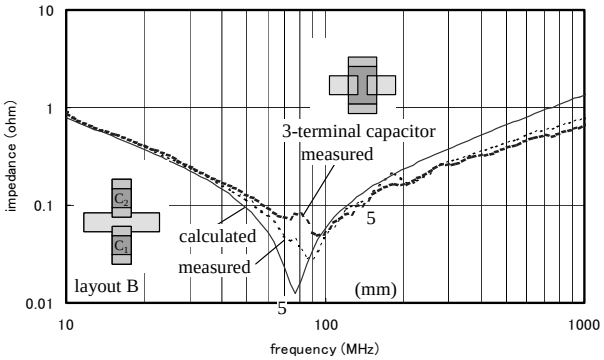


Fig. 13. Measured result when 3-terminal capacitor was used.

V. CONCLUSIONS

A simple technique to estimate the mutual inductance between capacitors when two bypass capacitors were used on the IC power supply was proposed. And a good agreement was obtained by comparing the calculated impedance of parallel capacitors by using estimated mutual inductance with the measured value.

The result by this technique showed the tendency that the opposite layout of the capacitors has more advantageous than side-by-side layout to lower the impedance. And it was confirmed that the 3-terminal capacitor has almost same effectiveness to opposite arranged two capacitors to decrease the impedance.

This presumption technique considers a capacitor as a thin wire, and it disregards width and the thickness of parts. Moreover, the influence of the via-hole and the pattern connected to capacitor are also not considered. Therefore, it seems that the presumption accuracy is comparatively low, and coverage is limited. However, because the calculation is easy, this technique is useful for the grasp of a general tendency when the layout of parts is considered.

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