Studying the Design and Performance of Conducted-Noise Spectrum Spreading in DC-DC Converters with an FPGA-Based Controller

Gamal M. Dousoky[#1] Masahito Shoyama[#2] Tamotsu Ninomiya[*3]

 # Electrical and Electronic Systems Engineering Department, Kyushu University
744 2-626-1 motooka, nishi-ku, Fukuoka, 819-0395 Japan
[1]gamal@ees.kyushu-u.ac.jp
[2]shoyama@ees.kyushu-u.ac.jp
[*] *Electrical and Electronic Engineering Department, Nagasaki University*
1-14 Bunkyo-machi, Nagasaki, 852-8521 Japan
[3]ninomiya@nagasaki-u.ac.jp

***Abstract*— This paper presents studying the design and performance of conducted-noise spectrum spreading in DC-DC converters. A novel technique for conducted-noise reduction has been proposed in this paper. The proposed technique uses three randomized parameters for generating the switching signals. These parameters are carrier frequency, duty-ratio, and the pulse position. This triple-hybrid spread-spectrum technique has been designed and implemented using field-programmable gate array (FPGA) technology.**
Moreover, the effect of using the proposed controller on both the conducted-noise and radiated-noise characteristics of the converter has been experimentally investigated. The experimental results show that using the proposed technique significantly improves the conducted-noise spectrum and effectively reduces the noise peaks at both high and low frequency ranges.

Key words: Noise Reduction, Random Switching, Spread Spectrum Techniques, EMI, EMC, FPGA.

I. Introduction

Switching power converters have been reported to generate common-mode and differential-mode conducted-noise in addition to radiated-noise. They may cause serious problems by generating such switching noise, [1]. This research aims to reduce the switching noise produced by DC-DC converters.

Pre-emptive electromagnetic interference (EMI) mitigation techniques eliminate the need for EMI filters by spreading the switching converters noise over a frequency range, [2]–[6]. By using these techniques, the noise generated by the switching power converters can be spread across frequency band. As a result, the average spectral power density of the broadband noise can thus be drastically reduced, [7].

FPGA is an attractive hardware design option. It has made substantial developments in many industrial control system applications, [8]. FPGA is much flexible than analog control, becoming lower cost, and applicable for power supply applications. The implementation of the triple-hybrid spread-spectrum technique has been achieved by using FPGA-based controller.

The paper is organized as follows: Section II presents triple-hybrid spread-spectrum technique which includes the design and implementation of the proposed FPGA-based. Section III describes the details of the experimental test circuit, results and discussion. Finally, conclusions have been presented in section IV.

II. Triple-Hybrid Spread-Spectrum Technique

A. The Basic Idea

According to Fig. 1, T_k is the duration of the kth cycle, α_k is the duration of the on-state within this cycle, and ε_k is the delay from the starting of the switching cycle to the turn-on within the cycle. Note that the duty ratio is $d_k= \alpha_k/ T_k$ and the switching frequency $F_k=1/T_k$. The switching function q(t) consists of a series of such switching cycles. In order to spread the frequency spectrum of the switching noise, $\{F_k, d_k,$ and\or $\varepsilon_k\}$ can be randomized.

Due to hardware limitations and the complexity of the control circuit, only one or two parameters could be randomized in the addressed techniques for power electronics applications, [2]–[6]. However, with the flexibility and programmability of the FPGA technology, all the three parameters have been randomized for generation the switching signal. This new hybrid technique has been designed, implemented and addressed in this paper.

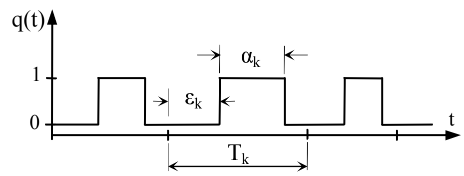


Fig. 1 Randomization parameters in the switching signal.

B. FPGA-Based Implementation

1. Pseudorandom Streams Generator

In order to spread the noise spectrum, {F_k, d_k, and ε_k} are randomized. Hence three random number generators are required to realize the proposed technique.

A pseudorandom streams generator has been constructed for this purpose. As shown in Fig. 2, the proposed construction uses several maximum length linear feedback shift registers (m-LFSRs) in parallel. For different m-LFSRs output bits, different initial contents of m-LFSRs (seeds) have been used. The taps are XOR'd sequentially with the output and then fed back into the leftmost bit.

The designed pseudorandom streams generator delivers three different random streams; (16-bit, 12-bit, and 10-bit streams). The streams are composed of the output bits of the m-LFSRs with different arrangements. The m-LFSRs are clocked regularly; i.e., the movement of the data in all the m-LFSRs is controlled by the same clock.

Only at the beginning of every switching cycle, the random output bits are converted into an integer numbers and used in the digital pulse-width modulator (DPWM). However, the other generated random output bits are discarded.

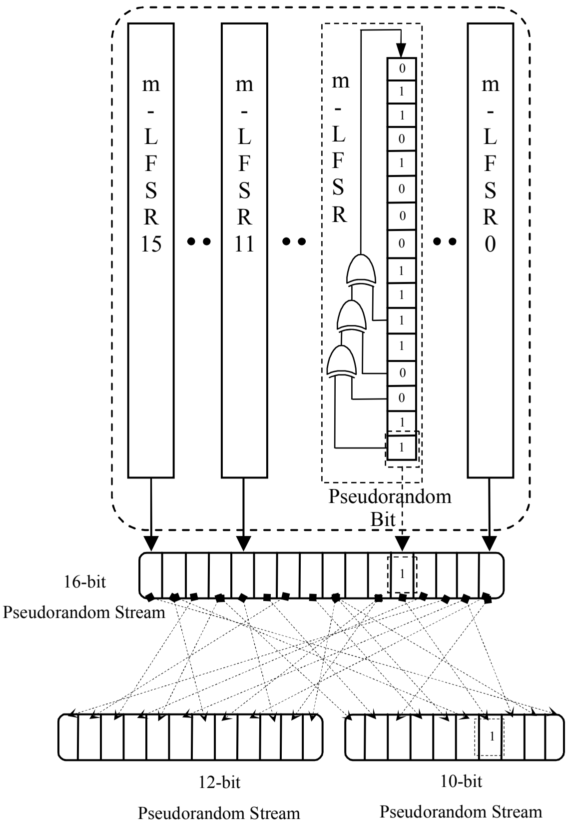


Fig. 2 The proposed pseudorandom streams generator.

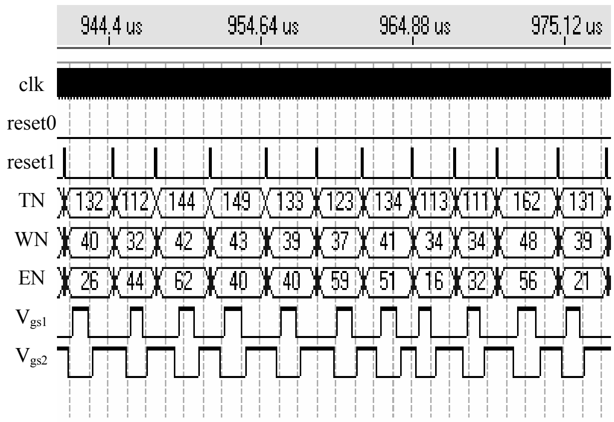


Fig. 3 VHDL simulation of the proposed FPGA-based controller for the proposed technique.

2. Digital Pulse-Width Modulator

At the beginning of every switching cycle, the DPWM achieves the following assignments:

1. Converting the pseudorandom streams into integer numbers.
2. Calculating randomization parameters for the started switching cycle and the needed number of steps to fulfill switching frequency, duty-ratio, and pulse position (TN, WN, and EN respectively as shown in Fig. 3).
3. Generating the digital pulse-width modulated waveforms ($Vgs_{1,2}$) with the commanded randomization parameters. As shown in Fig. 3, the designed DPWM uses a clocked-counter that increments and resets at the end of every switching cycle of the PWM (see reset1 signal).When the counter value lies between the reference values {EN, EN+WN}, the controller keeps the PWM output state high, else low. In this way, the digital pulse-width modulated waveforms ($Vgs_{1,2}$) are generated with the commanded randomization parameters.

III. Experimental Investigation and Results

The randomly switched converter has been designed and implemented using an Altera FPGA. A synchronous buck converter topology has been selected in order to improve efficiency and reduce heat loss. Fig. 4 illustrates the converter circuit configuration.

As described in Fig. 4 and Fig. 5a, the line impedance stabilization network (LISN) is used to standardize the input impedance seen from the converter input and sense the conducted-noise. A high-frequency current probe (C-Probe) is used to sense both the common-mode and differential-mode noise currents which are measured by an EMI receiver, [9]. The radiated-noise has been measured in a semi-anechoic chamber (SAC), as shown in Fig. 5b. The SAC is a shielded room having radio-frequency absorber material on the sides and at the top of the room to prevent reflections and simulate free space, [9]. Noise measurements have been taken at: V_{in} = 12 V, V_o = 3.3 V, I_o = 5 A, center switching frequency (f_{csw}=300 kHz), and center duty-ratio (d_{cdr}=0.275).

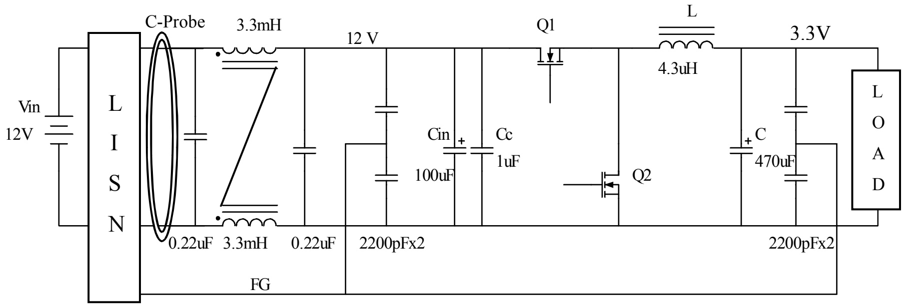


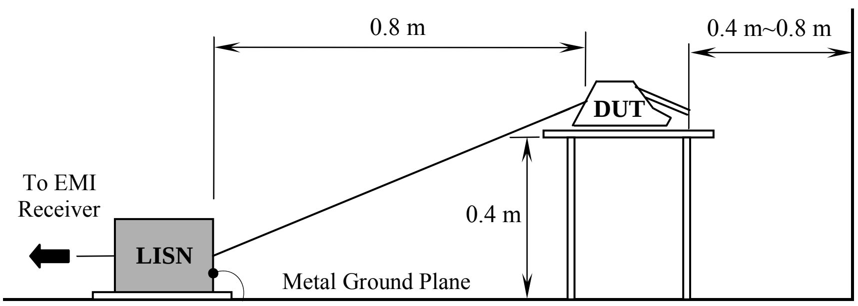
Fig. 4 Experimental converter circuit configuration.

Sweeping of the three randomization parameters has been carried-out for reaching the values which achieve the best conducted-noise spectrum spreading, as follows:

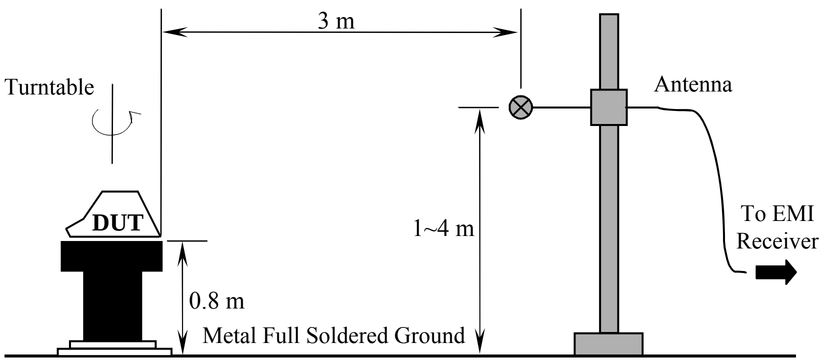
1. The switching frequency randomization ratio (ΔF_k), (0, ±10.92, ±21.85, and ±32.77 % of f_{csw} have been used).
2. The duty-ratio randomization ratio (Δd_k), (0, ±4.25, ±8.52, and ±17.05 % of d_{cdr} have been used).
3. The pulse position randomization ratio ($\Delta \varepsilon_k$), (0, 0.25~0.35, 0.2~0.4, and 0.1~0.51 of T_k have been used).

All the 64 studied cases have been designed, implemented and experimentally investigated. Then, the conducted-noise spectrums have been compared.

A comparison has been carried-out between all the studied cases for reaching the case which achieves the best conducted-noise spectrum spreading. Case 40 with the randomized parameters (RRRM, ΔF_k=±21.85% of f_{csw}, Δd_k=±4.25% of d_{cdr}, and $\Delta \varepsilon_k$=0.1~0.51of T_k) attains the best performance. It provides the highest conducted-noise peak reduction at the high and low frequency ranges. A shown in Fig. 6a and Fig. 7 the conducted-noise spectrum and its components have been significantly improved and the noise level has been effectively reduced. Moreover, the radiated-noise spectrum has been slightly improved by three decibels, as revealed in Fig. 6b.

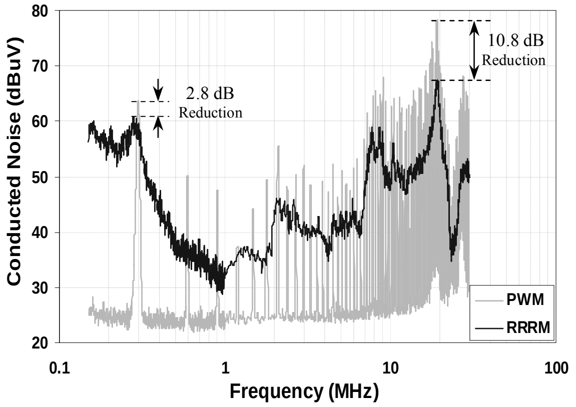


a) Conducted-noise test setup.

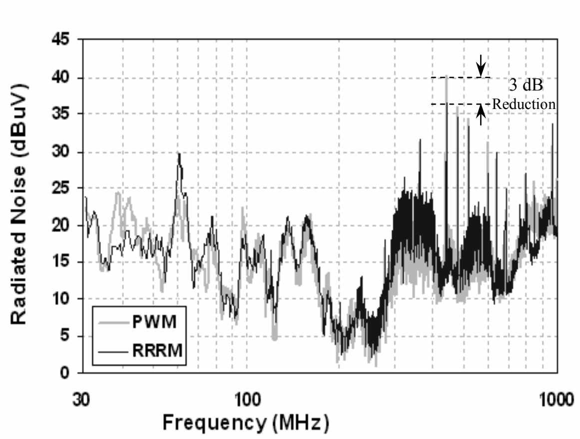


b) Radiated-noise test setup.

Fig. 5 Noise measurement system.

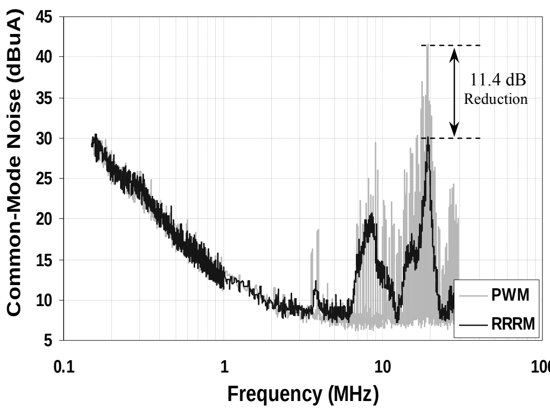


a) The measured conducted-noise spectrum.

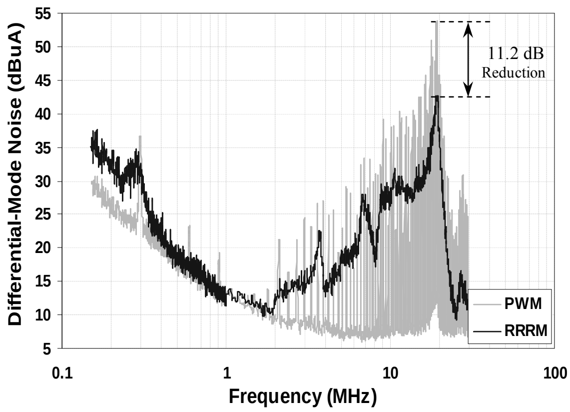


b) The measured radiated-noise spectrum with horizontal polarization.

Fig. 6 Comparison between the noise spectrum with the basic pulse-width modulation (PWM) and that with randomized parameters (RRRM, ΔF_k=±21.85% of f_{csw}, Δd_k=±4.25% of d_{cdr}, and $\Delta \varepsilon_k$=0.1~0.51of T_k).



a) Spectrum of common-mode noise current.



b) Spectrum of differential-mode noise current.

Fig. 7 Comparison between spectrums of the conducted-noise components with the basic pulse-width modulation (PWM) and that with randomized parameters (RRRM, ΔF_k=±21.85% of f_{csw}, Δd_k=±4.25% of d_{cdr}, and $\Delta \varepsilon_k$=0.1~0.51of T_k).

IV. Conclusions

A novel technique has been designed and implemented for conducted-noise reduction in DC-DC converters. Furthermore, the effect of using the proposed controller on both the conducted-noise and radiated-noise characteristics of the converter has been experimentally investigated. Finally, experimental results show that using the proposed technique, the conducted-noise spectrum has been significantly improved and the noise level has been effectively reduced. Moreover, the radiated-noise spectrum has been improved.

V. References

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