21PM1F-03

Optimization of Resistances in RL Snubbers for Power Distribution Network of Integrated Circuits

Ryosuke Yamagata [1], Kengo Iokibe [2], Yoshitaka Toyota [3]

[#] *Graduate School of Natural Science and Technology, Okayama University*
3-1-1 Tsushima-naka, Kita-ku, Okayama 700-8530 Japan
[1] yamagata@dev.cne.okayama-u.ac.jp
[2] iokibe@okayama-u.ac.jp
[3] toyota@okayama-u.ac.jp

Abstract— **Resonance of parasitic impedances in power distribution network (PDN) can increase leakage of the simultaneous switching noise current from integrated circuits (ICs) in the radio frequency (RF) range. The leaking SSN current is a major possible source of the conducted electromagnetic interference (EMI). A method have been proposed to control the PDN resonance by inserting a parallel RL circuit, RL snubber, to damp the resonance. In the previous work, the optimal resistance of the RL snubbers had been determined based on an equivalent circuit of PDN where equivalent series inductances (ESLs) on package had been neglected. In this work, the equivalent circuit was improved as the ESLs on package were taken into account because they were comparable to those on-board and not negligible. A method determining the optimal resistance was also improved. The RL snubbers were applied with the improved optimal resistance to a typical PDN. Effects of the RL snubbers in reducing the RF power current and in improving the power integrity were demonstrated in circuit simulations. Results of the demonstration confirmed that the improved method for optimal resistance gives more EMI reduction and better PI than the method in the previous work.**

I. Introduction

The design of the power distribution network (PDN) of modern integrated circuits (ICs) is becoming critical as the power supply voltage is lowered and as product size is getting smaller. The lower supply voltage requires designers to control the power bounce smaller. The product size becomes more compact, the intra-EMC issues become more critical.

The PDN is, in general, composed of multiple decoupling capacitors on-chip, on-package, and on-board[2]. The decoupling capacitors resonate with equivalent series inductances (ESLs) of the decoupling capacitors, traces, vias, and wires in PDN. The PDN resonance a possible cause of the power bounce and intra-EMC problems. Especially the resonance between on-chip capacitances and on-package and on-board ESLs is called 'mid-frequency resonance'[3][4]. In addition, another resonance can occur that is mainly due to parasitic capacitances between power and ground planes on board and on-board ESLs. These PDN resonances must be controlled to prevent ICs impairing their PI/EMC performances that may cause malfunctions.

To avoid such malfunctions due to the PDN resonance, PDN designers often reduce ESLs to shift resonant frequencies beyond the working frequency range of their target IC. But this is not a fundamental solution and could cause other problems in higher frequencies out of the working range.

A parallel RL circuit has been proposed in [1] to control EMI and PI performances by damping the PDN resonances. For designing the RL parallel circuit, a method to determine the optimal damping resistance was proposed. The proposed method was based on a simplified equivalent circuit specifying each PDN resonance. The equivalent circuit was simplified to a second-order circuit for the PDN resonance generated by capacitances and ESLs on-chip, on-package, on-board and a third-order circuit for the PDN resonance by on-board elements.

In this paper, the simplified equivalent circuit for the mid-frequency resonance is improved into a third-order circuit by taking on-package ESLs into account, which were neglected for ease of analysis. The optimal resistance will be determined with the third-order circuit and evaluated in terms of EMI and PI performances by comparing with results of the previous second-order equivalent circuit.

The RL parallel circuit was called RL damper in [1]. The same circuit was also applied to a dc-dc converter circuit and was called RL snubber in [6], in which it had suppressed broadband EMI due to a parasitic resonance in the dc-dc converter circuit. These two names, RL damper and RL snubber, are expressing the same circuitry and the latter name is RL snubber.

We determine the optimal resistance for the on-board resonance using the third order equivalent circuit. We will represent a common method to determine optimal resistance for both resonance#1(res#1) and res#2(res#2) in Section II. The RL snubbers will be validated with respect to reduction of the simultaneous switching current and input impedance of PDN numerically in Section III.

II. RL Snubber

We have proposed a method with RL parallel circuits to improve EMI and PI performances of ICs by damping the PDN resonances caused by shunt capacitances and ESLs distributed over a PDN. The RL parallel circuits, which are inserted series to power traces for damping the PDN resonances, are called RL snubbers. Snubber circuits have a function to suppress noises related to circuit resonances and are popular in the

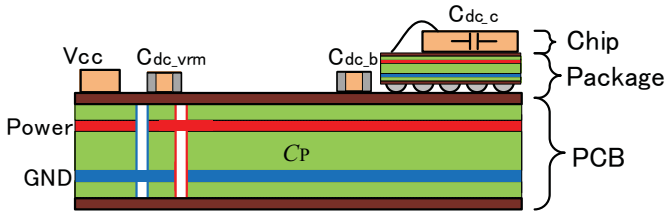


Fig. 1. Cross section diagram of PDN

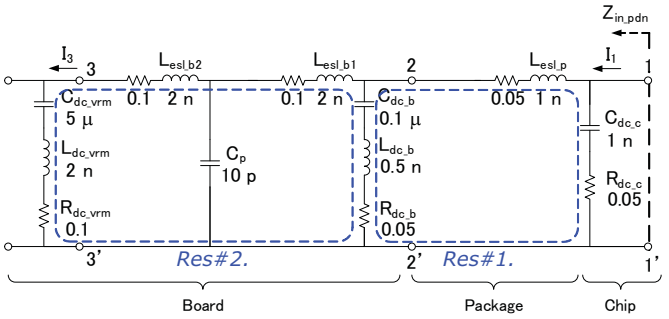


Fig. 2. Equivalent circuit of a typical PDN

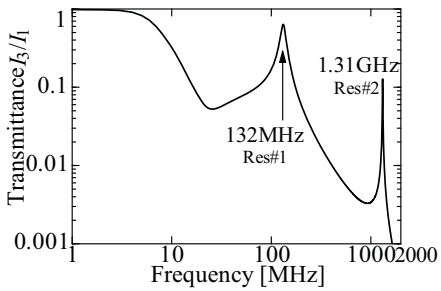


Fig. 3. Current transmittance of the PDN

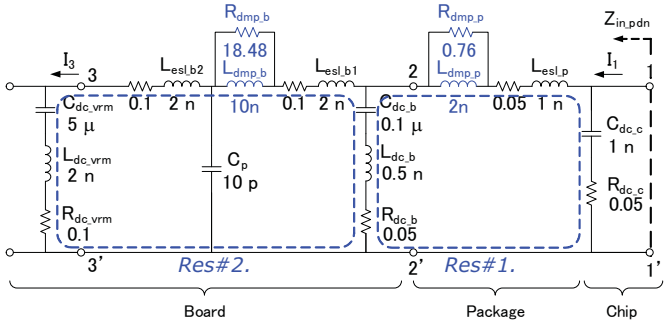


Fig. 4. Insertion of RL snubbers

fields of power electronics and EMC. Figure 1 illustrates a PDN composition over a stacked structure from a printed circuit board to a silicon chip. A decoupling capacitor $C_{\mathrm{dc\_b}}$ is mounted close to the IC package on board. A stabilization capacitor $C_{\mathrm{dc\_vrm}}$ is mounted near the VRM. The power and ground trace between IC and VRM, form a parallel plane pair and have a parasitic capacitance C_{p}(10 pF). Supposing that the IC has rather small scale, such as a microcontroller, and has no on-package decoupling capacitors, package impedance is dominated by ESLs of bonding wires and lines. There is $C_{\mathrm{dc\_c}}$ which value is 1 nF on chip. The value is considered parasitic capacitance. The equivalent circuit of this structure is shown in Fig. 2. A profile of transmittance of RF power current from port 1 to port 3, I_3/I_1 is shown in Fig. 3. Antiresonant peaks appeared at 132 MHz and 1.3 GHz. The resonance at 132 MHz, labeled as res#1, is caused by the chip capacitance $C_{\mathrm{dc\_c}}$ and inductances over PDN, and the other resonance, labeled as res#2, is resonance with C_{p}, and inductances over PDN. These resonances are caused by a shunt capacitance between power and ground traces, and ESLs distributed over PDN. A smaller shunt capacitance makes a higher resonant frequency.

Two RL snubbers are inserted onto the PDN as shown in Fig. 4. One is for res#1 and placed on package, the other for res#2 and on board. The snubber inductances on board and on package are set to be 10 nH and 2 nH, respectively. They are, respectively, 20 times and 6 times larger than $L_{\mathrm{dc\_b}}$. The on-board snubber inductance decouples the both sides of PDN across the on-board snubber, which limits ESLs that contributes to the res#1 to $L_{\mathrm{esl\_p}}$, $L_{\mathrm{dmp\_p}}$, and $L_{\mathrm{dc\_b}}$.

The on-package snubber inductance reduces contribution of $L_{\mathrm{esl\_p}}$ to res#2. These effects of snubber inductances simplify the equivalent circuit of PDN specializing for each resonance, as shown in Fig. 5.

A. For resonance#2

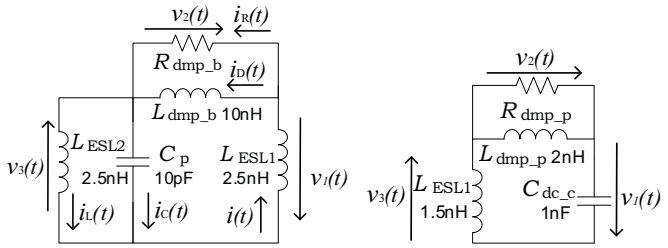
The circuit parameters in Fig. 5 are corresponding to those in the original PDN in Fig. 4. The inductance L_{ESL1} includes $L_{\mathrm{esl\_b1}}$ and $L_{\mathrm{dc\_b}}$. L_{ESL2} includes $L_{\mathrm{esl\_b2}}$ and $L_{\mathrm{dc\_vrm}}$. The decoupling capacitance at the voltage regulator module $C_{\mathrm{dc\_vrm}}$ is usually much larger than $C_{\mathrm{dc\_b}}$ and can be negligible, since its impedance is much smaller than that of $C_{\mathrm{dc\_b}}$. Other ESLs and resistances are omitted for ease of the following derivation of the optimal resistance.

The partial equivalent circuit for the res#2 is a third order RLC circuit. Transient response of second order RLC circuits depends on the discriminant of characteristic equation. If the discriminant is negative, the RLC circuit oscillates at a reduced frequency with an envelope gradually decreasing to zero. Else if the discriminant equals to or is greater than zero, input energy to the RLC circuit is damped without oscillation. Especially when the discriminant is zero, the system is damped as quickly as possible (critical damping).

In general, third-order circuits can be difficult to find out the resistance to realize the critical damping. In the case of the partial circuits illustrated PDN in Fig. 5, we could not find out such resistance of critical damping. In such a case, vibration searches for the state of converging early most. The optimal resistance is determined by drawing a root locus from a circuit equation.

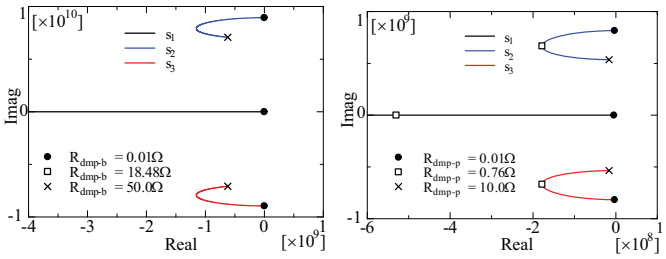
The derivation process of a characteristic equation in Fig 5(a) is shown below. Kirchhoff's voltage law gives

$$v_1 + v_2 + v_3 = 0. \tag{1}$$



(a) Res#2 (b) Res#1

Fig. 5. Simplified equivalent circuits related to resonances



(a) Res#2 (b) Res#1

Fig. 6. Root trajectory of the characteristic equation

Equation (1) is differentiated twice in time t,

$$\frac{d^2v_1}{dt^2} + \frac{d^2v_2}{dt^2} + \frac{d^2v_3}{dt^2} = 0. \tag{2}$$

Kirchhoff's current law gives

$$i = i_{\mathrm{R}} + i_{\mathrm{D}} = i_{\mathrm{C}} + i_{\mathrm{L}}. \tag{3}$$

Equation (3) is differentiated in time t,

$$\frac{di}{dt} = \frac{di_{\mathrm{R}}}{dt} + \frac{di_{\mathrm{D}}}{dt} = \frac{di_{\mathrm{C}}}{dt} + \frac{di_{\mathrm{L}}}{dt}. \tag{4}$$

Voltages across L_{ESL1}, L_{ESL2}, $L_{\mathrm{dmp\_b}}$ and $R_{\mathrm{dmp\_b}}$, and the current which flows through a C_{p} are denoted by the following equations,

$$v_1 = L_{\mathrm{ESL1}}\frac{di}{dt}, \tag{5a}$$

$$v_2 = R_{\mathrm{dmp\_b}}i_{\mathrm{R}}, \tag{5b}$$

$$v_2 = L_{\mathrm{dmp\_b}}\frac{di_{\mathrm{D}}}{dt}, \tag{5c}$$

$$i_{\mathrm{C}} = C_{\mathrm{P}}\frac{dv_3}{dt}. \tag{5d}$$

$$v_3 = L_{\mathrm{ESL2}}\frac{di_{\mathrm{L}}}{dt}, \tag{5e}$$

Equations (5a), (5b) and (5c) are substituted into Eq. (4) and it is solved in terms of v_1,

$$v_1 = \frac{L_{\mathrm{ESL1}}}{R}\frac{dv_2}{dt} + \frac{L_{\mathrm{ESL1}}}{L_{\mathrm{dmp\_b}}}v_2. \tag{6}$$

Equations (5b), (5c), (5d), and (5e) are substituted into Eq. (4) and it is solved in terms of v_3,

$$C_{\mathrm{P}}\frac{d^2v_3}{dt^2} + \frac{1}{L_{\mathrm{ESL2}}}v_3 = \frac{1}{R}\frac{dv_2}{dt} + \frac{1}{L_{\mathrm{dmp\_b}}}v_2. \tag{7}$$

Equations (1), (6) and (7) are rearranged about v_2. Replacing the derivative with s, the characteristic equation is expressed as,

$$\frac{C_{\mathrm{P}}L_{\mathrm{ESL1}}}{R_{\mathrm{dmp\_b}}}s^3 + \frac{C_{\mathrm{P}}(L_{\mathrm{ESL1}} + L_{\mathrm{dmp\_b}})}{L_{\mathrm{dmp\_b}}}s^2 + \frac{L_{\mathrm{ESL1}} + L_{\mathrm{ESL2}}}{L_{\mathrm{ESL2}}R_{\mathrm{dmp\_b}}}s + \frac{L_{\mathrm{ESL1}} + L_{\mathrm{ESL2}} + L_{\mathrm{dmp\_b}}}{L_{\mathrm{ESL2}}L_{\mathrm{dmp\_b}}} = 0. \tag{8}$$

where s is the complex frequency,

$$s = \sigma + j\omega. \tag{9}$$

TABLE I

RESISTANCES AND INDUCTANCES OF RL SNUBBER USED IN THE CIRCUIT SIMULATION

$R_{\mathrm{dmp\_b}}$	$L_{\mathrm{dmp\_b}}$	$R_{\mathrm{dmp\_p}}$	$L_{\mathrm{dmp\_p}}$
18.48 Ω	10 nH	0.76 Ω	2 nH

The trajectory of three root of the equation is plotted in Fig. 6(a) as varying $R_{\mathrm{dmp\_b}}$, which shows that Eq. (8) has one real root and complex conjugate roots. The transient response of the circuit in Fig. 5 vanishes fastest when the resistance $R_{\mathrm{dmp\_b}}$ is given as 18.48 Ω.

B. For resonance#1

An equivalent circuit of the partial circuit contributing to the res#1 is shown in Fig. 5(b) The characteristic equation of the equivalent circuit in Fig. 5 is

$$\frac{L_{\mathrm{ESL1}}}{R_{\mathrm{dmp\_p}}}s^3 + \frac{L_{\mathrm{ESL1}} + L_{\mathrm{dc\_p}}}{L_{\mathrm{dc\_p}}}s^2 + \frac{1}{R_{\mathrm{dmp\_p}}C_{\mathrm{dc\_c}}}s + \frac{1}{L_{\mathrm{dc\_p}}C_{\mathrm{dc\_c}}} = 0. \tag{10}$$

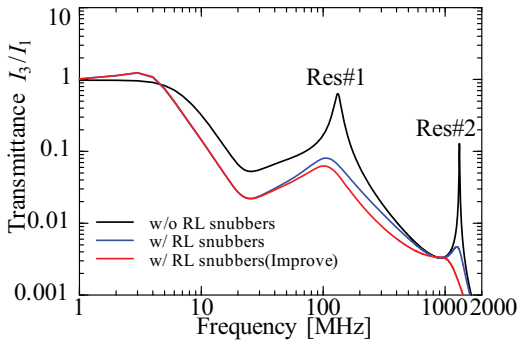
The trajectory of three root of the equation is plotted in Fig. 6(b) as varying $R_{\mathrm{dmp\_p}}$, which shows that Eq. (10) has one real root and complex conjugate roots. The transient response of the circuit in Fig. 5 vanishes fastest when the resistance $R_{\mathrm{dmp\_p}}$ is given as 0.76 Ω. The inductance $L_{\mathrm{dmp\_p}}$ was fixed as 2 nH here and was lower than $L_{\mathrm{dmp\_b}}$ for on-board damping keeping the PDN input impedance $Z_{\mathrm{in\_pdn}}$ rather low.

III. VALIDATIONS

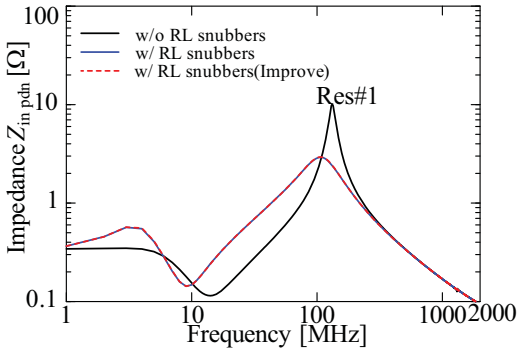
In this section, the proposed method is applied to power distribution networks of ICs in both numerical and experimental ways.

A. Circuit Simulation

Effects of the RL snubbers on EMI and PI will be validated with a commercial analog circuit simulator, AWR Microwave Office. The PDN analyzed is shown in Fig. 4. The parallel RL circuit was inserted both on-board and on-package power traces, quantities of which are listed in Table I. Results of the simulation, drawn in Fig. 7, are compared among three PDN configurations: (a) with RL snubbers the optimal resistance of which had been determined by the improved way, (b) with RL



(a) Current transmittance



(b) Input impedance of PDN

Fig. 7. Results of circuit simulations

snubbers by the previous way, and (c) without RL snubbers. When the black solid line of a graph does not insert RL snubber and a blue solid line inserts RL snubber using the resistance of paper [1], the case where a red solid line inserts RL snubber using the value of TABLE1 drawn in this paper is shown.

The EMI reduction effect the RL snubbers was measured by means of the simultaneous switching current. The current at Port 1 and Port 3 were observed and their ratio I_3/I_1, represented as 'current transmittance' bellow, were calculated. The calculated current transmittance are shown in Fig. 7(a). Sharp current peaks due to res#1 and res#2 are seen in the configuration without RL snubbers at 132 MHz and 1.3 GHz, respectively. The two sharp peaks were decreased in the configuration with RL snubbers. Furthermore, when the value of TABLE1 was used, the reduction effect was gained more.

We also investigated the other effect related to PI by means of the PDN input impedance $Z_{\text{in\_pdn}}$. Resultant $Z_{\text{in\_pdn}}$ shown in Fig. 7(b) indicates that (a) and (b) reduced more than the peak of (c) at 132 MHz. (a) and (b) increased the PDN impedance in the range below 100 MHz. But, it is not a problem because it is below target impedance. These results show that the RL snubbers are effective to improve PI performance by careful selection of the decoupling inductance on package.

IV. Conclusion

RL snubber, a method for damping PDN resonances, was investigated for better EMI and PI performances of digital integrated circuits. The method for determining the optimal resistance of the RL snubber was improved. In the previous literature, the method had been based on a second-order equivalent circuit of PDN, in which on-package ESLs had been neglected. The second-order equivalent circuit had been derived for looking into the PDN resonance due to a parasitic capacitance between on-board power and ground traces. Since the on-package ESLs on package was not negligible, the equivalent circuit for the on-board PDN resonance took the on-package ESLs into account and was became third order circuit. The characteristic equation of the improved equivalent circuit was derived and its root trajectories were plotted as the resistance of the snubber varied. The root trajectories indicated that the characteristic equation had a complex conjugate root and a real root, which means that the resistance giving the real part of the complex root, the time constant, minimum makes the transient response of PDN to the simultaneous switching noise damped fastest. The fastest damping also occurs in power bounce and conducted power current. Thus the resistance of the fastest damping was decided as the optimal resistance. RL snubbers with such optimal resistances was applied to a PDN. We confirmed that the improved method for determining optimal resistance provided better EMI reduction than that in our previous work and that it gave as same PI performance as the previous work.

References

[1] K. Iokibe, Y. Yano, and Y. Toyota, "Insertion of Parallel RL Circuits into Power Distribution Network for Simultaneous Switching Current Reduction and Power Integrity" 2012 Asia-Pacific International Symposium on Electromagnetic Compatibility in Singapore. (APEMC 2012). pp. 417-420 May. 2012.

[2] L. D. Smith, R. E. Anderson, D. W. Forehand, T. J. Pelc, and T. Roy, "Power distribution system design methodology and capacitor selection for modem cmos technology," IEEE Trans. Adv. Packag., vol. 22, no. 3, pp. 284-291, 1999.

[3] B. Garben, R. Frech, J. Supper, and M. F. McAllister, "Frequency dependencies of power noise," IEEE Trans. Adv. Packag., vol. 25, no. 2, pp. 166-173, 2002.

[4] W. Becker, J. Eckhardt, R. Frech, G. Katopis, E. Klink, M. McAllister, T. McNamara, P. Muench, S. Richter, and H. Smith, "Modeling, simulation, and measurement of mid-frequency simultaneous switching noise in computer systems," IEEE Trans. on Comp., Packag, Manufact. Technol. B, vol. 21, no. 2, pp. 157-163, 1998.

[5] IEC61967-6, Measurement of RF currents, Magnetic Probe Method. IEC 47A/568/CD, 1999.

[6] K. Kam et. al, "Method to Suppress the Parasitic Resonance Using Parallel Resistor and Inductor Combination to Reduce Broadband Noise form DC/DC Converter," EMC'09/Kyoto, 22Q2-4, Kyoto, Japan, Aug. 2009