21PM1E-04

Prototype of 3-Gb/s 60-GHz Millimeter-wave-based Wireless File-transfer System

Yasuo Asakura [#1], Keitarou Kondou [#2], Masashi Shinagawa [#3], Shinya Tamonoki [#4], Makoto Noda [#5]

[#] *Device Solutions Business Group, Sony Corporation*
5-1-12 Kitashinagawa, Shinagawa-ku, Tokyo, Japan

[1] YasuoA.Asakura@jp.sony.com
[2] Keitarou.Kondou@jp.sony.com
[3] Masashi.Shinagawa@jp.sony.com
[4] Shinya.Tamonoki@jp.sony.com
[5] MakotoB.Noda@jp.sony.com

Abstract—**We report the development of the prototype of a high-speed wireless file-transfer system using a 60-GHz band. The prototype achieved an effective user-data rate over 3 Gb/s using a quadrature-phase-shift keying modulation, including overheads of a physical layer and a retransmission control between two memory devices, by using a new 40-nm CMOS baseband LSI and automatic direct memory-access control.**

I. Introduction

Recently, many 60-GHz millimeter-wave-based wireless systems have been standardized, such as IEEE802.15.3c [1], IEEE802.11ad [2], ECMA-387 [3], and ISO/IEC 13156 [4]. Many applications for such standards have been proposed [5], including high-definition (HD) video streaming, file transfer, wireless docking station, gaming, short-range backhaul, wireless desktop, and wireless Gigabit Ethernet.

However, at present, there are only two commercial applications for 60-GHz wireless systems: short-range backhaul using an original format [6] and HD video streaming using WirelessHD [7] for a television that is an industry standard. One obstacle to the application of a 60-GHz wireless system for other usages, such as file transfer for a mobile, is the high power consumption of the system. To address this problem, we recently reported a low-power radio frequency (RF) and baseband (BB) solution [8] using a rate 14/15 low-density parity-check (LDPC) code [9][10] and a high-speed parallel digital timing and carrier recovery (DCTR) [11]. Another obstacle is that the effective data rate of interfaces (I/Fs) employed in current mobile, such as smart phones and tablets, is relatively low, below 100 Mb/s in most cases, compared with a data rate of more than 2 Gb/s in a 60-GHz wireless system. Thus, the total data rate is limited by the data rate of the I/F employed when a 60-GHz wireless system is connected to the I/F.

In this study, we demonstrate a fast file-transfer system with an effective user data rate of more than 3 Gb/s between two memories, based on the usage model proposed.

II. Usage Model and Demonstration

There exist usage models that do not require a data rate for the I/F employed in a mobile higher than the data rate of a wireless device connected to the I/F. Fig. 1 shows one such usage model supposed in this study in which a user downloads contents, such as a movie, and then plays them. While downloading (left side of Fig. 1), the maximum possible data rate between the memory in a PC or Kiosk and the memory in a mobile is preferred. This usage is known as "sync and go." For playing content (top right in Fig. 1), the data rate required can be much lower than that required for downloading because most of the content is compressed. Uncompressed HD-video streaming usage (bottom right in Fig. 1) is common for a 60-GHz wireless system, but power consumption, around 3 W of a current commercial system should be reduced below 1 W, is required for a mobile.

Fig. 2 shows a photograph of a demonstration of a 3-Gb/s wireless file-transfer system using the developed prototype. A transmitter (Tx) is mounted under the tablet and a receiver (Rx) is mounted under the laptop PC. The prototype consists of a newly developed control module, a BB LSI that has been improved based on that of [8], and a 60-GHz direct-conversion RF LSI that is identical to that of [8] connected to two end-fire radiation antennae [12].

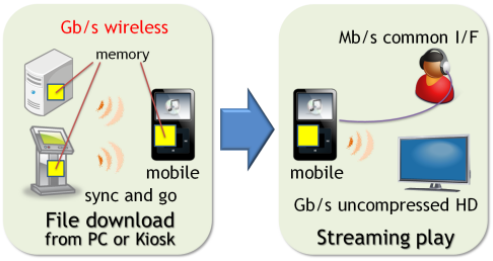


Fig. 1. Usage model supposed in this paper

Fig. 2. Photograph demonstrating a 3-Gb/s wireless file-transfer system using the developed prototype

III. System Configuration

A. File Transfer Scheme

Fig. 3 shows the data flow in conventional file transfer in which a transceiver is directly connected to an application I/F [13]. When a transceiver is used as a Tx for file transfer in Fig. 3, the CPU sends file data a_1 in random access memory (RAM) to an I/F host through the internal bus of the application, then the I/F host sends file data a_2 in the I/F format to a wireless media-access controller (MAC) through I/F. The wireless MAC send file data a_3 in the wireless-system format to a wireless physical layer (PHY). When a transceiver is used as an Rx for file transfer, as shown in Fig. 3, the data flow is reversed, except that an I/F device is used to substitute for the I/F host.

Note that an effective data rate of a_2 is usually much slower than that of a_3 for a 60-GHz wireless transceiver because the internal bus is controlled by a CPU with a large latency. Therefore, an effective data rate of a_3 is limited to an effective data rate of a_2.

To avoid this problem of rate mismatch, a system using direct memory access has been reported [14]. However, the difficulty in realizing direct memory access is that there is no approach to avoid a conflict of memory access by a host selected from multiple host candidates for memory. Because a memory can be read or written by one memory host at a time, either an application or a transceiver, some method of control for switching between hosts is required to avoid the conflict. When a memory host in an application is switched to that in a transceiver, the memory host in an application usually cannot recognize any modification of files in the memory by the transceiver. This is because a file allocation table (FAT) is usually retrieved only once by a memory host in an application at the beginning of the connection in many common I/Fs such as a USB.

To avoid this problem of a memory-access conflict, some control schemes for switching between memory hosts have been proposed [15][16]. These systems, however, have a problem in that the switching time is relatively long because host switching is manually controlled by a user. Therefore, we have developed an automatic direct memory-access control based on wireless-packet information.

Fig. 4 shows a block diagram of the transceiver in Fig. 2. In Fig. 4, the PC or tablet sends file data using a USB 3.0 PHY I/F (defined in USB-standard) [17] as I/F in Fig. 3 to a USB PHY and control data to a micro controller (CTRL). A USB PHY sends USB-packetized file data, d_1, to a USB MAC, and then USB MAC converts d_1 to parallelized file data, d_2. A micro CTRL sends the parallelized control data of a transceiver, c, to a Bridge CTRL that supplies ctrl signals to the USB 3.0 MAC, the memory-access CTRL, a wireless MAC, and a BB LSI. The memory-access CTRL sends file data, d_3, using DDR SDRAM I/F to an 8-GB DRAM. Although volatile DRAM is employed as cache memory in this study, non-volatile memory such as a flash memory would be preferable as a commercial product to improve user's convenience. Wireless MAC packetizes d_2 to a packet signal, d_4, and transmits d_4 to a BB LSI with a data rate

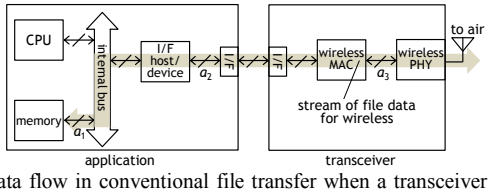


Fig. 3. Data flow in conventional file transfer when a transceiver is directly connected to an application I/F.

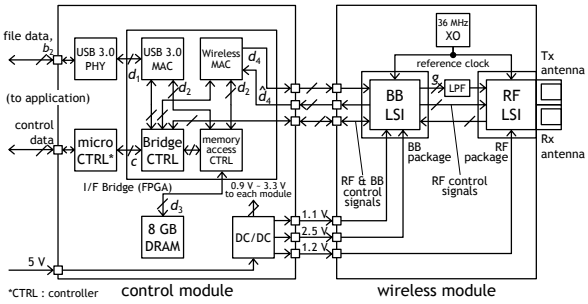


Fig. 4. Block diagram of the transceiver shown in Fig. 2

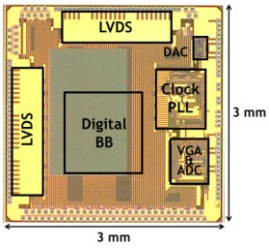


Fig. 5. Die micrograph of the new 40-nm CMOS BB LSI shown in Fig. 4

determined by the modulation scheme employed. The BB LSI in a 10.0 mm × 10.0 mm package converts d_4 into an analog-BB signal, g, then an RF LSI in a 16.3 mm × 14.4 mm package converts g up to the 60-GHz band. The 60-GHz band signal from an Rx antenna is converted to file data in reverse order.

Employing a USB Mass Storage Class for USB MAC and the newly developed automatic direct memory-access control enables a wireless file transfer without I/F-specific driver software. Although an FPGA is employed for developing the I/F Bridge in Fig. 4, the circuit in the FPGA would be implemented into a BB LSI for a commercial product.

B. BB LSI

Fig. 5 shows a die micrograph of the new 3.0 mm × 3.0 mm 40-nm CMOS BB LSI in Fig. 4. The BB LSI in this study is very similar to that in [8], but resolves some implementation problems of the former BB LSI: (1) the new LSI takes a reference-clock frequency of 36 MHz, which is the same as that for RF LSI generating a symbol rate, f_s, of 1728 mega sample/s (MS/s), while the former one took 35 MHz generating f_s of 1680 MS/s; (2) the new LSI can use the full range of a 6-bit digital-to-analog converter (DAC), while the former one used only half the range because of the digital-to-analog I/F mismatch; and (3) the new LSI enables an auto-gain controller (AGC) by employing the new analog BB in [18], while the former AGC did not work well because of an unexpected oscillation of VGA above a gain of 20 dB.

Fig. 6 shows a block diagram of the BB LSI in Fig. 4. In the Tx shown in Fig. 6, Tx packet data, h_1, are LDPC encoded to coded data, h_2, and a Golay preamble and synchronization

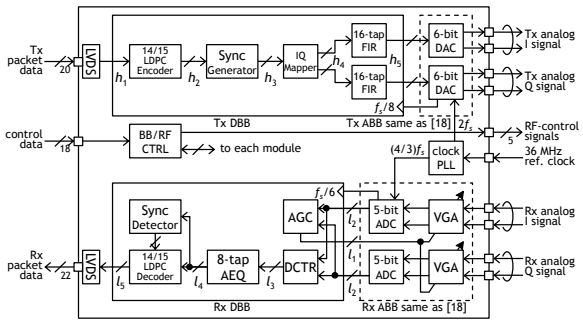


Fig. 6. Block diagram of the BB LSI shown in Fig. 4

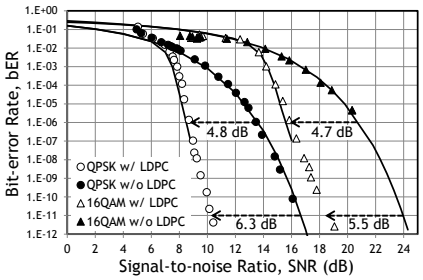


Fig. 7. Experimental bER as a function of SNR with and without LDPC code for QPSK and 16QAM by a loopback condition connecting a Tx BB to Rx BB without RF LSI

patterns are inserted into h_2 by a sync generator. Then the preamble concatenated into coded data, h_3, is converted to a digital-modulated signal, h_4, by an IQ mapper followed by 16-tap finite-impulse response (FIR) filters that equalize the spectrum of h_4 as satisfying a 60-GHz spectral mask [1]–[3] for a 2.16-GHz bandwidth/channel, and DACs convert digital equalized signal, h_5, to analog I/Q signals. In the Rx shown in Fig. 6, the input analog signal is converted to a digital signal through VGA and 5-bit ADC, and the asynchronously sampled ADC output, l_2, is converted to a carrier-and-timing recovered signal, l_3, by DCTR [11] without using a pilot word. Then l_3 is equalized by an 8-tap adaptive equalizer (AEQ), whose tap weights are obtained by an least-mean squares algorithm; a sync detector synchronizes the packet and the LDPC decoder correct errors of demodulated l_4 to obtain an estimated h_1, l_5. Here, the AGC automatically controls VGA by a gain-control signal, l_1, so as to maintain the level of ADC output to a predetermined value within 0.5 μs from the reception of a data packet. Three modulations are available for the BB LSI, *i. e.* π/2-shift binary-phase shift keying modulation (BPSK), π/2-shift quadrature-phase-shift keying modulation (QPSK), and 16-quadrature amplitude modulation (16QAM). The channel-bit rates are 1.728 Gb/s for BPSK, 3.456 Gb/s for QPSK, and 6.912 Gb/s for 16QAM. Power consumptions excluding that of I/O for the BB LSI were 126 mW for QPSK and 138 mW for 16QAM in Tx, 268 mW for QPSK and 292 mW for 16QAM at bER below 10^{-12}, and 299 mW for QPSK and 319 mW for 16QAM at bER of 10^{-6} in Rx

Fig. 7 shows the experimental bit-error rate (bER) as a function of the signal-to-noise ratio (SNR) with and without a rate-14/15 LDPC code [1][10] for QPSK and 16QAM by a loopback condition connecting a Tx BB to Rx BB without RF LSI, where the solid lines show theoretical bER without LDPC and simulated bER with LDPC under the additive white Gaussian noise (AWGN) channel. Here, SNR is defined as $20\cdot\log(s/\sigma)$, where s is an averaged signal level and σ^2 is a variance of signal errors. The maximum number of iteration for an LDPC decoder was 8 for QPSK and 3 for 16QAM. No error floor was observed for the LDPC decoder in Fig. 7.

Although the loop back condition can achieve bER below 10^{-11} for 16QAM, currently bER of the system for 16QAM is around 10^{-3} which is not sufficient for robust implementation of a system in which RF LSI is connected to BB LSI as described in [8]. Therefore, our system is currently used for QPSK and BPSK.

IV. Performance Evaluations

A. Radiation characteristic as a system

Fig. 8 shows a perspective view of a wireless module in Fig. 4, that is, antennae and an RF LSI in a package on a printed-circuit board in a chassis. A horizontal Tx-antenna angle, θ_t, a vertical Tx-antenna angle, φ_t, a horizontal Rx-antenna angle, θ_r, and a vertical Rx-antenna angle, φ_r, for indicating antenna direction are also shown in the figure. Although the size of the chassis is currently very large, it was used for the first evaluation to obtain the effect of a chassis on an antenna.

Our system employs single 6-dBi antenna [12] with end-fire radiation for Tx and Rx. A radiation pattern designed as having a half-radiation power of ±30° of the antenna had been clarified, but the radiation pattern of an antenna as a wireless module has not been clarified.

Fig. 9 shows the experimental and theoretical relationships between the relative power of a received signal and the radiated angle of the Tx antenna: (a) in the horizontal plane

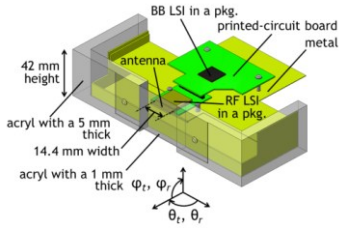
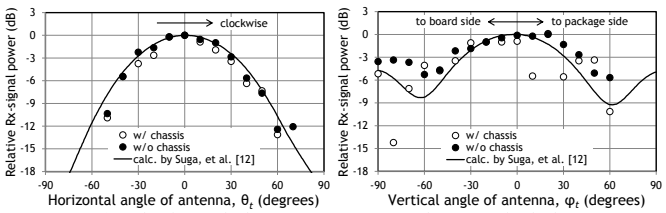
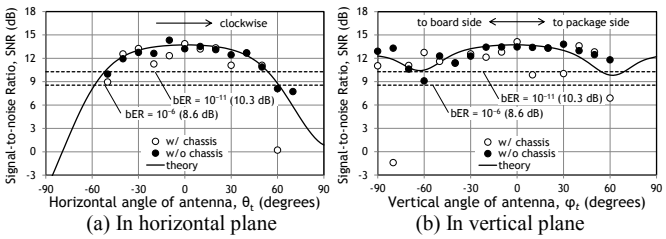


Fig. 8. Perspective view of a wireless module in Fig. 4



(a) In horizontal plane (b) In vertical plane

Fig. 9. Experimental and theoretical relationships between relative power of received signal and radiated angle of Tx antenna



(a) In horizontal plane (b) In vertical plane

Fig. 10. Experimental and theoretical relationships between SNR(θ_t, φ_t) and radiated angle of Tx antenna

and (b) in the vertical plane. In Fig. 9, 0 dB is defined as the power at the angle showing the maximum value in the experimental condition without a chassis, and the solid lines are quoted from [12]. The experimental plots in Fig. 9 were evaluated at $\theta_r = 0$, $\varphi_r = 0$, the distance between Tx and Rx as 40 cm, and the modulation of QPSK in an anechoic chamber.

Fig. 10 shows the experimental and theoretical relationships between the SNR(θ_t, φ_t) and the radiated angle of Tx antenna: (a) in the horizontal plane and (b) in the vertical plane. The experimental condition for Fig. 10 is the same as that for Fig. 9. The dashed lines in Fig. 10 are the thresholds to obtain bER of 10^{-6} and 10^{-11}. The maximum transmission distance to obtain bER of 10^{-6} was 2.0 m.

In Fig. 10, we obtained the theoretical relationship between SNR(θ_t, φ_t) and antenna angle as follows:

$$\mathrm{SNR}(\theta_t, \varphi_t) = \mathrm{SNR}_{Tx} - 10 \cdot \log\left(1 + \frac{r_n}{g_t(\theta_t, \varphi_t)^2 \cdot g_r(\theta_r, \varphi_r)^2}\right), \quad (1)$$

where r_n is a noise power ratio defined as $(\sigma_r/(\sigma_t \cdot g_p))^2$, $g_t(\theta_t, \varphi_t)$ is a gain of Tx antenna isotropic given in [12], $g_r(\theta_r, \varphi_r)$ is a gain of Rx antenna fixed to $g_r(0, 0)$ in this study, and SNR_{Tx} is the SNR of Tx defined as $20 \cdot \log(s_t/\sigma_t)$, where s_t is an averaged signal level at an input of Tx antenna, σ_r^2 and σ_t^2 are variances of signal errors for Rx and Tx, respectively, and g_p is a propagation loss. SNR_{Tx} of 14.7 dB and $r_n/g_r(0, 0)^2$ of 0.250 are used for fits of experimental plots in Fig. 10.

Theoretical results in Fig. 9 and Fig. 10 showed relatively a good agreement with their experimental results; however, some deterioration was observed in experimental results with chassis at a large angle because of reflection. From Fig. 10, it is clarified that ranges of angle to obtain below bER of 10^{-6} are 103° (from −52° to 50°) in horizontal axis and 129° (from −56° to 72°) in vertical axis at the given distance of 40 cm.

B. File transfer

For demonstrating low redundancy of the proposed system, which means that effective user-data rate is close to channel-data rate of 3.5 Gb/s using QPSK and 1.7 Gb/s using BPSK, the effective user-data rate was measured.

Fig. 11 compares measured and calculated packet-error rate (PER) dependence of an effective user-data rate, r_e.

In Fig. 11, we obtained r_e using the following equation:

$$r_e = \frac{r_s \cdot l_p}{t_p + t_e + 2\mathrm{SIFS} + \frac{\mathrm{PER}}{1 - \mathrm{PER}} \cdot (t_p + \mathrm{RIFS})}, \quad (2)$$

where r_s of 1 is a time occupancy rate for the wireless file transfer in a duration of a Superframe, l_p of 829440 bits is a length of a file-data packet, t_p of 2.6×10^{-4} s for QPSK and 5.2×10^{-4} s for BPSK are a duration of the file-data packet, t_e of 2.6×10^{-6} s is a duration of an acknowledgment (ACK) packet, SIFS of 2.5×10^{-6} s is a short inter-frame space, and RIFS of 9.0×10^{-6} s is a retransmission inter-frame space. Wireless MAC in this study employs a re-transmission protocol that is based on the immediate ACK policy of IEEE 802.15.3c [1], and the definitions of Superframe, SIFS, and RIFS are the same as those of the standard.

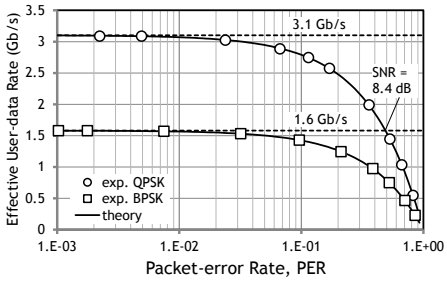


Fig. 11. Relationship of data rate and PER in the proposed system

In Fig. 11, we notice that the maximum data rate of 3.1 Gb/s using QPSK, which is only 10 % loss of the channel-bit rate, was achieved in our demonstration and we should use BPSK when SNR for QPSK is lower than 8.4 dB.

ACKNOWLEDGMENT

A part of this work was financially supported by the Research and Development Project for Expansion of Radio Spectrum Resources of the Japanese Ministry of International Affairs and Communications. The authors are grateful to Prof. M. Ando and Dr. K. Fukuzawa of Tokyo Institute of Technology (TITECH) for their encouragements in this project. The authors thank Prof. A. Matsuzawa and Assis. Prof. M. Miyahara for providing VGA, ADC, and DAC, Assoc. Prof. K. Okada for providing an RF LSI, and Dr. Y. Hirachi for providing antenna in a package, each of TITECH. The authors also thank Mr. H. Ino of Sony for supporting to take radiation characteristics and Mr. H. Yamagishi of Sony for discussing about a wireless communication.

REFERENCES

[1] *Wireless MAC and PHY Spec. for High Rate Wireless Personal Area Networks (WPANs) Amendment 2: Millimeter-wave-based Alternative Physical Layer Extension*, IEEE Std. 802.15.3c, 2009.
[2] *Wireless LAN MAC and PHY Spec. - Amendment 3: Enhancements for Very High Throughput in the 60 GHz Band*, IEEE Std. 802.11ad, 2012.
[3] *High Rate 60 GHz PHY, MAC and PALs*, Standard ECMA-387, 2010.
[4] *Info. Tech. -- Telecomm. and Info. Exchange between Systems -- High rate 60 GHz PHY, MAC and PALs*, ISO/IEC 13156, 2011.
[5] IEEE Standard Association, "802.15.3c Usage Model Document (UMD), Draft," 802.15.3c DCN 55, 2007.
[6] BridgeWave Communications, Inc., [Online]. Available: http://www.bridgewave.com/products/60ghz.cfm
[7] WirelessHD, [Online]. Available: http://www.wirelesshd.org/
[8] K. Okada, *et al.*, "A Full 4-Channel 6.3Gb/s 60GHz Direct-Conversion Transceiver With Low-Power Analog and Digital Baseband Circuitry," in *ISSCC Dig. Tech. Papers*, pp. 218-219, Feb. 2012.
[9] M. Noda, "Designing a Self-orthogonal Quasi-cyclic Code with Extended Minimum Hamming Distance," in *Proc. IEEE Turbo Coding*, Apr. 2006.
[10] H. Yamagishi and M. Noda, "High Throughput Hardware Architecture for (1440, 1344) Low-density Parity-check Code utilizing Quasi-cyclic Structure," in *Proc. IEEE Turbo Coding*, pp. 78-83, Sep. 2008.
[11] K. Kondou and M. Noda, "A New Parallel Algorithm for Full-digital Phase-locked Loop for High-throughput Carrier and Timing Recovery Systems," in *Proc. IEEE ICECS*, pp. 1156-1159, Dec. 2010.
[12] R. Suga, *et al.*, "A Small Package With 46-dB Isolation Between Tx and Rx Antennas Suitable for 60-GHz WPAN Module," *IEEE Trans. Microwave Theory and Tech.*, vol.60, no.3, pp. 640-646, Mar. 2012.
[13] *Wireless Universal Serial Bus Spec.*, Rev. 1.1, Chapter 8, 2010.
[14] A. Estrada, "Method and System for Transferring Data between Wireless Devices," U.S. Patent Application 12/687,064, Jan. 2010.
[15] L. Yao, Japanese utility model, 3109346, 2005.
[16] T. Konno, Y. Aoki, K. Tsutsui, and N. Adachi, "Card-type Peripheral Device," U.S. Patent 7 925 812, Apr. 12, 2011.
[17] *Universal Serial Bus 3.0 Spec.*, 2011.
[18] M. Miyahara, *et al.*, "An 84 mW 0.36 mm^2 Analog Baseband Circuits for 60 GHz Wireless Transceiver in 40 nm CMOS," in *Proc. IEEE RFIC Symp.*, pp. 495-498, Jun. 2012.