On Chip Transformer Design for CMOS Power Amplifiers

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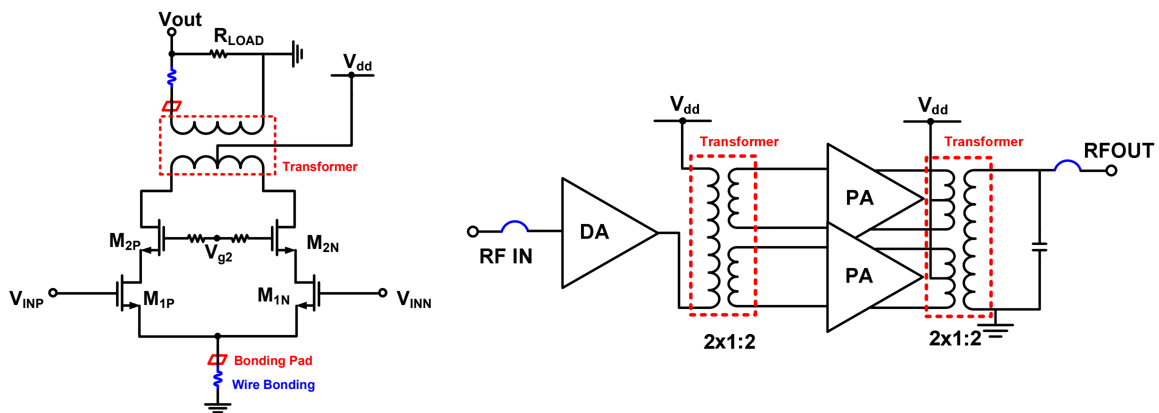
1. Introduction

CMOS technology has been widely applied to the design of RF circuits by advantage of low cost, compact size and high system-on-chip integration capability. But the high power amplifier is undesirable building block for CMOS process due to the low breakdown voltage of gate oxide[1]. This problem becomes more serious as the minimum gate lengths are scaled down in each new process generation. The other problem associated with the design of on-chip power amplifiers using CMOS processes is the high loss of on-chip impedance transformation [2]. This is caused by the highly conductive substrate, as well as thin metal and dielectric layers. Recently, many literatures have been presented CMOS power amplifiers in wireless communications comparable to other process ones. The breakdown voltage is one of the inherited drawbacks of CMOS transistor, so typical CMOS power amplifiers adapted the cascode type differential structure as in figure 1 to relieve the voltage stress at the output. Due to the limitation of the output voltage swing, the optimum load for the power cell should be minimized. Also, its structure inevitably needs differential to single-ended conversion at output stage[3].



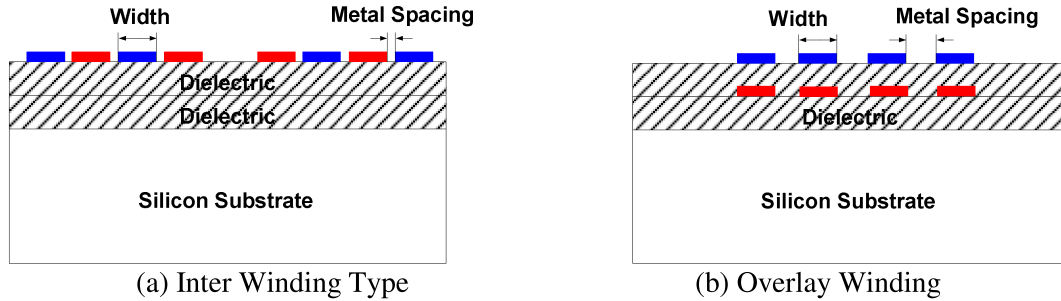
(a) Cascode type differential power amplifier schematic (b) Conventional power amplifier system
Figure 1: Typical CMOS Power Amplifiers with On Chip Transformer

In this work, we proposed on chip transformer targeted to around 900 MHz WCDMA application. At these frequencies, small size and low loss impedance transformation is challengeable task. The transformer was fabricated by standard 0.18 μm RF CMOS process which support two thickest top metals.

2. Monolithic Transformer

The on chip transformer in CMOS power amplifiers plays two roles. First, it transforms the 50 Ω output load into optimum impedance. Second, it converts the differential signal to a single-

ended signal so that it can be connected to the antenna directly. The advantage of the magnetically coupled transformer is its compact size and the low insertion loss which is independent of the impedance-transformation ratio.
Typical transformer is that two parallel conductors are interwound in the same top plane as shown in figure 2.(a). It used edge coupling of the magnetic field between windings[4]. Normal CMOS process supports thickest top metal which is typically 4~5 times thicker than other metal layers. The thick top metal exhibits the smallest sheet resistance. It is helpful to enhance the Q value of the transformer. The disadvantages of the design are that the coupling factor is limited by the minimum spacing rule of the design process and the Q value of the conductors are degraded by wide metal width for current density.



(a) Inter Winding Type (b) Overlay Winding

Figure 2: Cross Section of Monolithic Transformer Configuration

Multiple conductor layers can be used to fabricate broadside coupled transformer as illustrated in figure 2.(b). This implementation was first described by Finlay for spiral inductors[5]. The advantages of this type winding are reduced physical area and enhanced coupling factor. Although the windings are identical, asymmetry in the electrical response is happened by sheet resistance difference between the metal layers thickness. The parasitic capacitances of each winding also differ because of the distance from the substrate and the shielding effect of top winding by overlapped lowers. In addition, parallel capacitance between windings limits the frequency response.

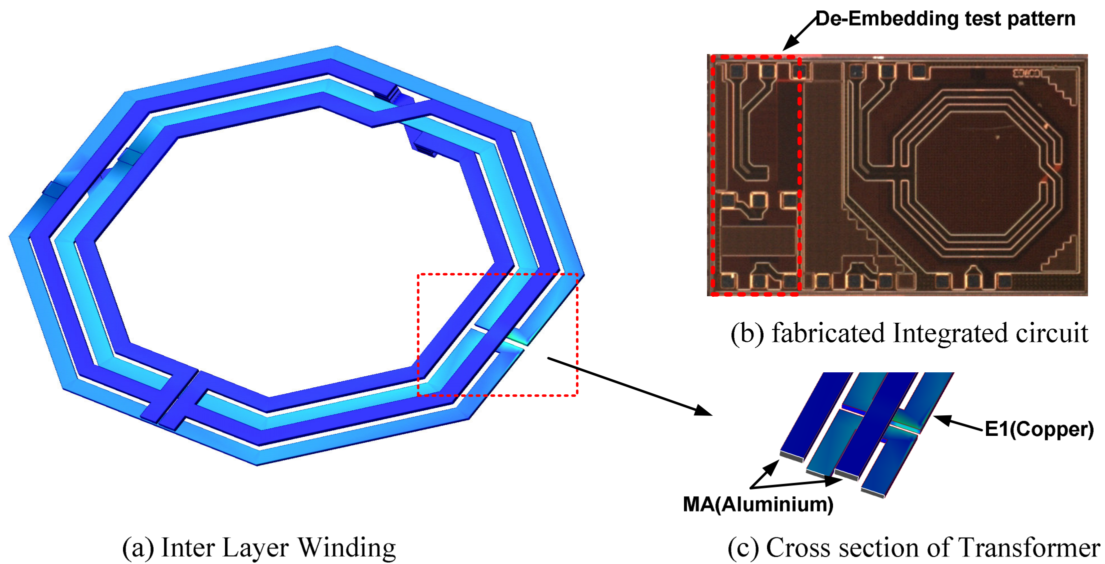
Table 1: Process Characteristics

Technology	IBM 0.18 μm CMOS
Top metal sheet resistance(MA)	7 mΩ /square
Top metal thickness	4 μm (Aluminium)
Second top metal sheet resistance(E1)	6.3 mΩ /square
Second top metal thickness	3 μm (Copper)
Substrate thickness	300 μm
Thin metal sheet resistance (Mx, x=2,3,4,5)	89 mΩ /square
Thin metal thickness (Mx, x=2,3,4,5)	0.48 μm (Aluminium)

3. On Chip Transformer Design

The proposed on chip transformer uses IBM 0.18 μm CMOS process which support two thickest upper metal layers in the seven metals as in table 1. The thicknesses of the aluminium and copper layers of upper two metals are 4 μm and 3 μm, respectively. They show over 10 times smaller sheet resistances than other layers.
Aluminium is the standard material used to fabricate the metallization layers of integrated CMOS circuits. Many fabrication process vendors support thick aluminium top layer. Most on chip RF inductors are supplied by top metals. Copper has superior material characteristics to Aluminium. The copper resistivity is 0.0179 $\Omega mm^2/m$ (20 ℃), while the resistivity of the aluminium is 0.028

$\Omega mm^2/m$ (20 ºC). It requires particular technology to obtain its deposition on silicon substrates. So it is rarely supported from vendors. Especially top copper metal, it is hard to find normal CMOS process. Clearly, the Cu process has a lower series resistance even though it has 1 μm smaller thickness. The slight discrepancy between upper two metals can be overcome by adopting proposed structure as in figure 3. The two windings located at each layer to form a transformer. Each one turn winding consists of two 30 μm width conductors based on octagonal transformer. This structure is simple to design and scale with frequency. The outer diameter of E1 layer winding is 870 μm.



(a) Inter Layer Winding (c) Cross section of Transformer

Figure 3: Proposed Transformer Architecture

The two windings are located separate layers, the minimum distance rule of same layer can be neglected. It also use edge and parts of wide side coupling, the coupling factor of proposed structure can be higher than inter winding type. The horizontal distance of proposed transformer is shorter than inter winding type. It has a merit of size issue. Compared to overlay type, this structure is free from shielding effect and parallel capacitance. To improve the magnetic coupling, slight overlapping between windings can be helpful unless the parallel capacitance severely increase.

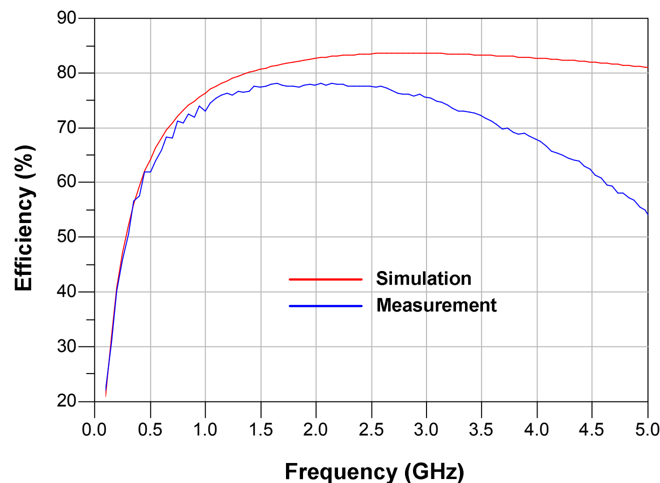


Figure 4: Efficiency of Proposed Transformer

4. Experimental Results

The 1:1 inter layer winding type transformer with a 5 μm horizontal conductor spacing has been fabricated and tested. For the simulation, Agilent ADS™ Momentum was used. It is an 2.5-D

electromagnetic simulation tool that calculates S-parameters of a given planar structure. It can easily model standard microstrip or slotline topologies. The inter windings parallel capacitance introduced by closely spaced conductor is acceptable during conductor space tuning.
Figure 4 shows the simulated and measured results of the transformer efficiency. The efficiency calculated from the maximum available gain to check the loss of transformer itself, which shows the loss of optimally matched transformer. From Figure 4, a good agreement can be found between simulation and measurement until 2 GHz. The discrepancy above 2 GHz should be analyzed in future work. The measured efficiency of this power combining transformer is about 75 % at 900 MHz, this can be applicable CMOS power amplifiers instead external transformer with wire bonding or power combining components.

5. Conclusion

A inter layer winding type transformer was proposed. At target operation frequency of 900 MHz, the measured efficiency of the proposed transformer is about 75%. In addition, the test shows good agreement between simulated and measured results. The transformer allows full integration of impedance transformation and differential to single combining with comparable size and performances.

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