PROCEEDINGS OF ISAP '96, CHIBA, JAPAN

A Study on Arrival Paths in Wide-band Mobile Communication Systems

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1. INTRODUCTION

In such wide-band mobile communication systems as CDMA systems, it is possible to improve communication quality by using a RAKE receiver that effectively combines the powers of multipath components. It is clear that there will be many independent paths which are combined by RAKE receivers when a higher chip rate is selected. However, the resultant performance of the RAKE receiver will rather degrade if the chip rate is too high. This is because the reception power is diversified to too many paths and accordingly the power captured by the limited number of RAKE receiver taps becomes small. Thus, for the development of RAKE receivers, it is necessary to investigate the characteristics of resolvable multipath components[1]. Narrow-band and wide-band CDMA systems are now under development [2]-[4]. However, the most suitable bandwidth for CDMA systems has not been determined yet.

This paper investigates the relationship between the chip rate that is related to the band width and the number of available paths for a RAKE receiver, based on the measured power delay profiles. The relationship between the number of RAKE receiver taps and the powers captured by a RAKE receiver was also studied.

2. AVAILABLE PATH

Figure 1 shows a typical example of power delay profiles. We define an available path, i.e. the path which produces a reception power within ΔL(dB) below the maximum reception power as shown in Fig.1(b). Power delay profiles can be presented as two models : one is the instantaneous power delay profile, the other is the short term power delay profile to which instantaneous delay profiles are averaged by every ΔD distance. In this paper, we evaluate the characteristics using the short term power delay profile.

3. MEASUREMENT

The experiment was carried out in urban areas of Tokyo by using a correlating detection method[5]. In these areas, there are a lot of tall buildings with 5 -15 stories and propagation paths are not line of sight. Table 1 shows the experimental parameters. The carrier frequency is at the 2.6GHz band and the transmitter power is 6W. The base station antenna is a corner reflector antenna with 60° beam width and placed on the top of the building at 71m height. The mobile antenna is a colinear antenna and placed on the roof of the measurement car at 2.9m height. Short term power delay profiles were obtained every 10m by averaging instantaneous power delay profiles measured every 1m distance. The maximum excess delay is 30μs, which corresponds to a traveled distance of 9 km.

4. ANALYSIS OF SHORT TERM AVAILABLE PATH

Figures 2 (a)-(c) show the relationship between the loss of path with maximum reception power and the number of available paths. The value of ΔL is 6dB, and the figures are for chip rates of 7.5, 15, and 30Mchip/s respectively. In all cases, the number of available paths increases as the loss of path with maximum reception power increases. A larger loss of path with maximum reception power generally means a long distance between base and mobile stations. Therefore the number of arriving paths necessarily increases. When the loss of path with maximum reception power is large, the number of available paths increases as the chip rate becomes high.

Figures 3 (a)-(c) show the cumulative distribution of the number of available paths, for chip rates of 7.5, 15, and 30Mchip/s respectively. The value of ΔL is 6dB. The broken lines are the cumulative distribution in the whole area and the solid lines are that where the loss of path with maximum reception power exceeds 145dB. For chip rates of 7.5, 15, and 30Mchip/s, the number of available paths at the cumulative probability of 50% is 3, 3, and 5 respectively in the whole area and 6, 8, and 10 respectively in the area where the loss of path with maximum reception power exceeds 145dB.

Figure 4 shows the relationship between the chip rate and the number of available paths with the parameter ΔL. When $\Delta L = 3$dB, the number of available paths at the cumulative probability of 50% is 3 or more when the chip rate exceeds 7.5Mchip/s.

5. ANALYSIS OF RAKE RECEIVER TAP

In the previous section, we described the number of available paths. This helps to determine the number of RAKE receiver taps. This section describes the receiver performance when the number of RAKE receiver taps is fixed to a value.

Figure 5 shows an algorithm of a RAKE receiver. The number of RAKE receiver taps is assumed as k. In this algorithm, k highest path powers are combined. The power of the path with maximum reception power is P_{max} and the power captured by the RAKE receiver with k taps is P_{rake}. Figure 6 shows the captured power P_{rake} normalized by P_{max} when the chip rate is 15Mchip/s and the number of RAKE receiver taps is k=5. The relative power P_{rake}/P_{max} increases as the loss of path with maximum reception power increases. This is because the number of available paths increases as the loss increases as shown in Fig. 2.

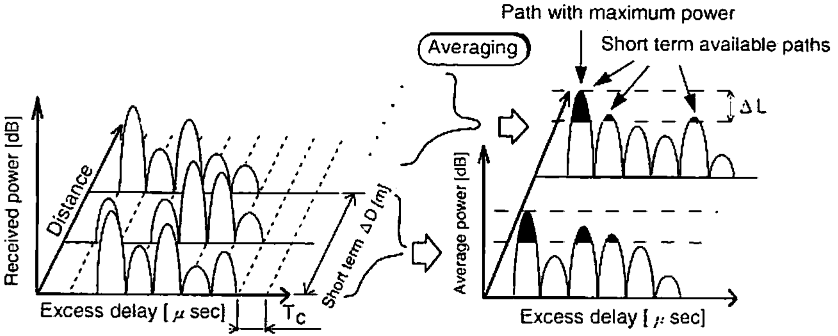
Figure 7 shows the relationship between the loss of path with maximum reception power and P_{rake}/P_{max} as a parameter of the RAKE receiver taps k. Here P_{rake}/P_{max} is given as a value at the cumulative probability of 50% of P_{rake}/P_{max} where the loss of path with maximum reception power exceeds 145dB. The relative power P_{rake}/P_{max} increases as the chip rate becomes high. 5 taps RAKE exceeds the value of P_{max} by about 4 dB at 5Mchip/s and by about 5dB at 7.5Mchip/s or higher. As compared to 5 taps RAKE, 10 taps RAKE further gains by about 1dB at 5Mchip/s and by about 2dB at 7.5Mchip/s or higher.

6. CONCLUSION

The relationship between the chip rate and the number of available paths and that between the number of RAKE receiver taps and the power captured by a RAKE receiver were clarified in urban areas. It also became clear that both the number of available paths and the captured power by a RAKE receiver increase especially as the chip rate increases in areas where the loss of path with maximum reception power is higher.

REFERENCE

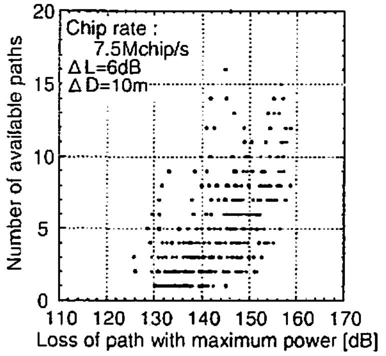
[1] S. A. Allpress et al.: "An Investigation of RAKE Receiver Operation in an Urban Environment for Various Spreading Bandwidth Allocation", Proc. of IEEE VTC, pp. 506-510, 1992.
[2] K.S. Gilhousen et al.: "On the capacity of a cellular CDMA system". IEEE Trans. Veh. Technol., VT-40, 1972.
[3] PG. Andermo, G. Brismark : "CODIT", Atestbed project evaluating DS-CDMA for UMTS/FPLMTS", Proc. of IEEE VTC, pp. 21-25, 1994.
[4] K. Ohno et al. : "Wideband coherent DS-CDMA", Proc.of IEEE VTC, pp.779-783, 1995.
[5] D. C. Cox : "Delay Doppler characteristics on multipath propagation at 910MHz in suburban mobile radio environment", IEEE Trans. Antennas and Prapagat., AP-20, pp. 625-635, 1972.



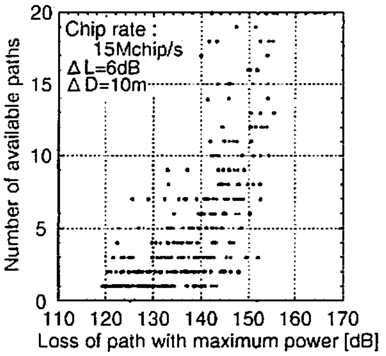
(a) Instantaneous delay profile

(b) Short term delay profile

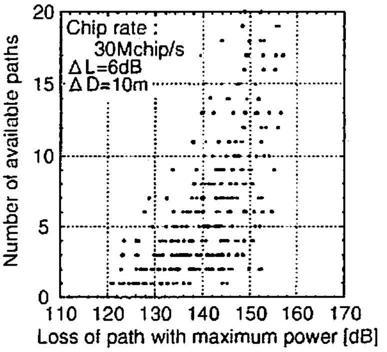
Fig.1 Delay profile model



(a) 7.5Mchip/s

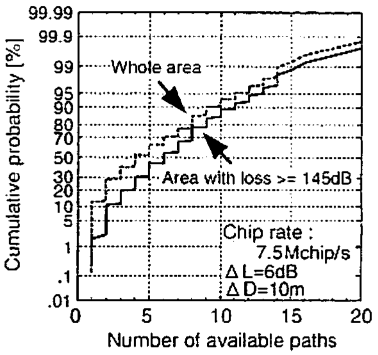


(b) 15Mchip/s

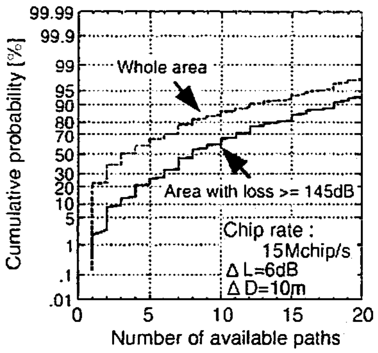


(c) 30Mchip/s

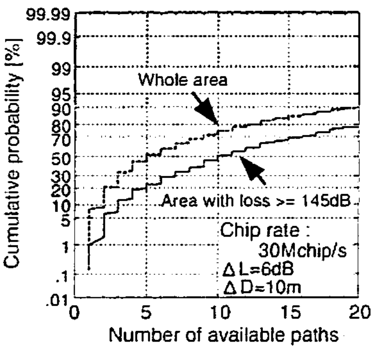
Fig.2 Loss of path with maximum power and number of available paths



(a) 7.5Mchip/s



(b) 15Mchip/s



(c) 30Mchip/s

Fig.3 Cumulative distribution of available paths

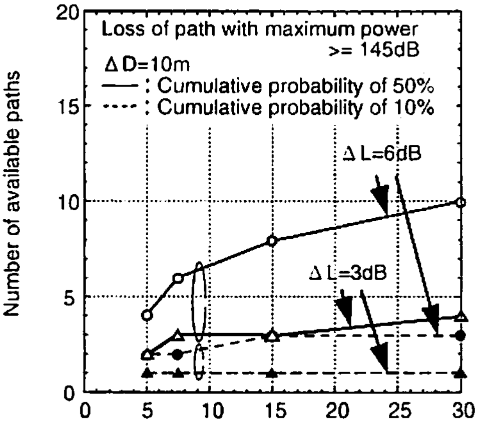


Fig.4 Chip rate and number of available paths

Table1 Major parameters of experiment

Frequency	2.598 GHz
Modulation	BPSK modulated by 1023-bit pseudorandom binary sequence
Chip rate	5, 7.5, 15, and 30 Mchip/s
Transmitter power	6 w
Antenna height of base station	71 m
Antenna height of mobile station	2.9 m

< Number of available paths = k >

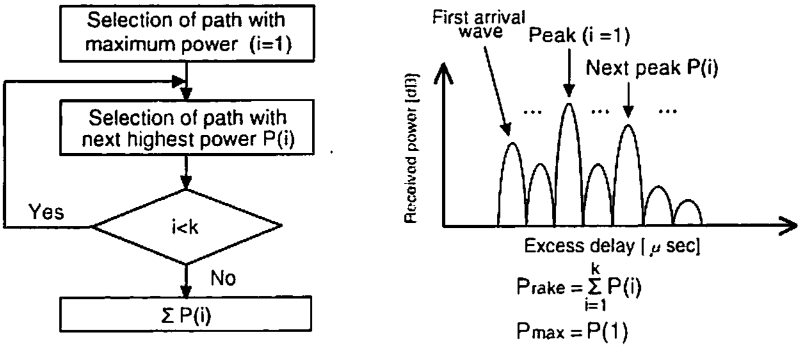


Fig.5 Algorithm of RAKE receiver

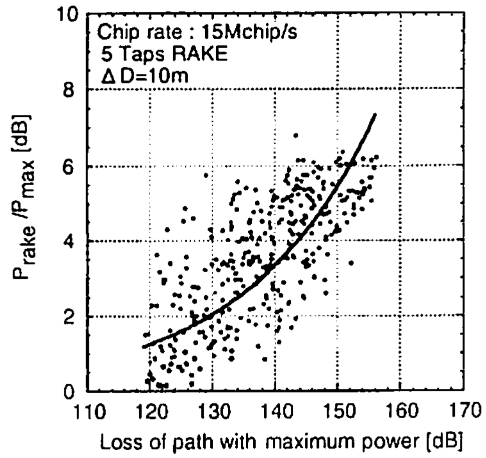


Fig.6 Loss of path with maximum power and P_{rake}/P_{max}

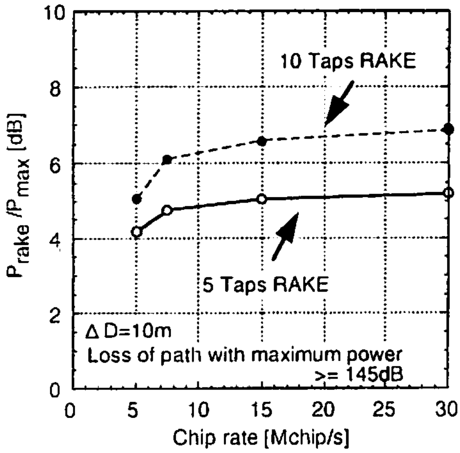


Fig.7 Chip rate and P_{rake}/P_{max} at Cumulative probability of 50%