Quantitative Evaluation of Common-Mode Radiation from a PCB Based on Imbalance Difference Model

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Abstract: We have evaluated a major source of EMI, the common-mode on a multi-layer printed circuit board (PCB), using a method based on the "imbalance difference" mechanism which we developed for the EMC design of PCB layouts. Calculation by our method is much faster than ordinary calculations because of the two-phase modeling scheme; i.e., separate evaluations of the excitation voltage and a common-mode antenna. In this paper, we evaluate the effect of guard traces on a narrow ground plane with our method as an example of suppressing common-mode radiation. The calculated suppression is compared to measured values to verify the effectiveness of the method.
Key words: EMI, common-mode radiation, printed circuit board, ground plane, imbalance difference

1. Introduction

Evaluation and reduction of the common-mode radiation from a printed circuit board (PCB) are of practical importance in reducing EMI. A high-speed device on a PCB drives a normal-mode functional signal, and it unintentionally couples to the common-mode current, which causes significant EMI at certain resonances of the structure.

The structure shown in Fig. 1 is very common among practical PCBs; one or more high-speed signal traces run either above a narrow ground plane or close to the edge of a ground plane. It is well known that the ground pattern under the signal trace

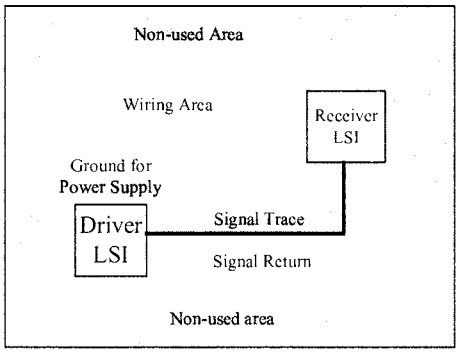

Fig. 1 Limited ground connection on a PCB.

plays an important role as a current return path and also as the reference potential for signals. Thus, a microstrip structure requires a wide ground pattern for signal integrity and EMI control. When signal traces are routed in the vicinity of a ground-plane edge or run on a narrow ground plane, the common mode is generated because of the reference voltage fluctuation – in other words, normal mode to common mode conversion occurs.

In many papers, this common-mode generation has been regarded as caused by the ground inductance, and the mechanism has been called "current-driven" [1] because the voltage fluctuation is proportional to the product of the ground inductance L_G and the time-derivative of the normal-mode current di_N/dt. However, evaluation of the ground inductance for a practical PCB is not easy. Therefore, the common-mode generation has usually been calculated directly through a full-wave electromagnetic simulation such as the FD-TD method [2], which is generally very time-consuming.

We have proposed an alternative mechanism based on the mismatch of a PCB's transmission line imbalance [3-6]. According to this mechanism, the common-mode generation can be modeled in two phases – evaluation of the excitation source voltage and evaluation of the common-mode antenna. Each evaluation requires only a short calculation time, so we can control and repeatedly verify design parameters in a PCB layout design to obtain a result that meets design requirements.

In this paper, we summarize the generation mechanism and describe an example of a low-EMI PCB design procedure. To demonstrate the validity of our method, we compare obtained results with measured values.

2. Features of the Design Scheme

2.1 Mechanism of Common-Mode Generation

For a PCB with a narrow ground pattern, we have developed a common-mode generation scheme [3] by using a parameter called the current division factor (CDF). This parameter expresses the degree of transmission line imbalance.

The CDF, denoted as h, is derived from the cross-section of a transmission line, and the common-mode voltage (V_C) is described as

$$V_C(x,f) = V_R(x,f) + h(x)\, V_N(x,f), \qquad (1)$$

where x, f, V_N, and V_R denote, respectively, the position along the line, frequency, normal-mode voltage, and return trace voltage. As Eq. (1) shows, the common-mode voltage depends on the CDF.

In this approach, we focus on discontinuous points of transmission line structures as shown in Fig. 2(a). The difference in the imbalance excites the whole PCB and generates common-mode radiation. In most cases, the CDF values for the two sides (h_a, h_b) will differ because of the difference in the imbalances of the transmission lines, and the common-mode voltages for the two sides will also differ. The difference (ΔV_C) acts as a common-mode driving voltage, which is proportional to the difference between the imbalances:

$$\Delta V_C(x,f) = (h_b - h_a)\, V_N(x,f). \qquad (2)$$

The common-mode current is excited by the driving voltage in the common-mode equivalent circuit, which consists of a combination of the signal trace, the return plane, and the system ground. If a PCB is located far from other metal objects, the common-mode equivalent circuit acts as an antenna which we call a common-mode antenna (Fig. 2(b)). If we excite this common-mode antenna with a unit voltage source, we can obtain the antenna radiation factor through numerical analysis. We denote this factor as $\mathbf{F}(\mathbf{r},f)$, where $\mathbf{r}$ is the position vector of the observation point.

We can then calculate the common-mode radiation by the equation,

$$\mathbf{E}(\mathbf{r},f) = \Delta V_C(x',f)\, \mathbf{F}(\mathbf{r},f) = (h_b - h_a)\, V_N(x',f)\, \mathbf{F}(\mathbf{r},f). \qquad (3)$$

From Eq. (3), the radiated emission is the product of the imbalance difference, the normal-mode voltage, and the antenna radiation factor.

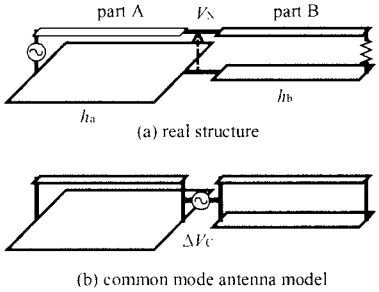

Fig. 2 Imbalance difference model.

2.3 Amount of Calculation

Next, we will discuss the amount of calculation. The above calculation is much faster than three-dimensional full-wave electromagnetic calculations such as the FD-TD method, in which small meshes are usually used to divide the PCB structures. In Eq. (3), we use three factors – the normal mode voltage, the CDF difference, and the antenna radiation factor.

The method to calculate antenna radiation is the same as the commonly used antenna calculation method; however, the mesh size can be much larger. The ordinary numerical calculation uses meshes which should be smaller than the line dimensions, signal trace width, dielectric thickness, and so on. In contrast, the common-mode antenna does not require small meshes since the transmission line structure in the antenna model can be ignored. This is because most of the common-mode current flows on the return plane. The shape of the common-mode antenna is dependent only on the ground plane shape. Therefore, the mesh size for a common-mode antenna is usually larger than that of the traditional method by a factor of ten. If we use the FD-TD method for antenna calculation, the amount of calculation is proportional to the inverse fourth power of the mesh size. Thus, our calculation for the common-mode antenna is faster than that for the traditional method by a factor of 10^4.

The calculation of normal-mode voltage is usually much faster than the antenna calculation. This voltage is usually calculated for SI. So, no additional calculation is needed.

The calculation of CDF is done through an electrostatic field analysis of a cross-section of the transmission line structure [4]. We use the boundary element method (BEM) for this analysis. This calculation is two-dimensional, so it usually takes less than ten seconds with a personal computer.

In the PCB design procedure, we often need to control the interconnection structures on a PCB to obtain a sufficiently low EMI. In other words, we only evaluate the radiation difference when changing local transmission line structures. In this case, only the CDF calculation is needed. We will show an example of this in the next section.

3. Example of a Low-EMI Design

3.1 Test PCB

Figure 3 shows our test PCB. This PCB was based on the simplified model from Fig. 1. It has a signal trace driven by a driver module. The driver consists of a CMOS buffer (74AC00), a clock oscillator, and a voltage regulator. The load is matched to the line impedance (75 Ω). This PCB is two-layered. The bottom layer (the shaded area in Fig. 3) is a ground plane.

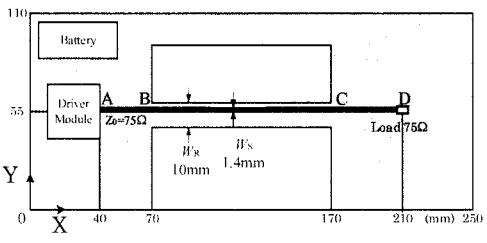

Fig. 3 Schematic of the test PCB

3.2 Common-Mode Antenna Model

In Fig. 3, points B and C are where the transmission line structures change, so the value of CDF along the line changes at these points. The common-mode driving forces are generated at these points, and the common-mode antenna is as shown in Fig. 4. We denote the driving forces at points B and C as V_{C1} and V_{C2}, respectively. They are calculated as

$$V_{C1} = (h_{BC} - h_{AB})V_{NB} \quad (4a)$$

$$V_{C2} = (h_{CD} - h_{BC})V_{NC}, \quad (4b)$$

where h_{AB}, h_{BC}, and h_{CD} are the CDFs for sections AB, BC, and CD, respectively, and V_{NB} and V_{NC} are the normal-mode voltage at points B and C, respectively.

The CDF for an ideal microstrip structure is 0. We regard h_{AB} and h_{CD} as 0, because the return plane widths of sections AB and CD are sufficiently wide. Equations (4a) and (4b) indicate that the common-mode driving forces are proportional to h_{BC}. Therefore, a low-EMI design is equivalent to a decrease of h_{BC}.

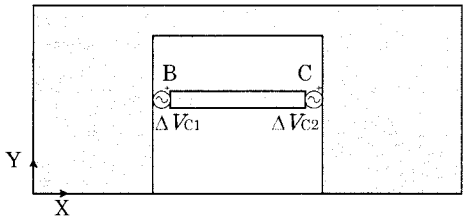

Fig. 4 The common-mode antenna model.

3.3 Modified Structure

In general, effective ways to decrease CDF for a microstrip structure are to use a wide return plane, use a guard trace, move the signal trace towards the center of the return plane, and so on. In this study, we used guard traces. We considered six types of test PCBs:

(1) without a guard trace.
(2) with an outside guard trace.
(3) with an inside guard trace.
(4) with a guard trace on both sides.
(5) with an outside guard trace with impedance matching.
(6) with a guard trace on both sides with impedance matching.

The signal trace at section BC is located close to the ground plane edge. We refer to the side near the ground edge as 'outside', and the other side as 'inside' as shown in Fig.5. In this study, the guard trace width was fixed as equal to the signal trace width (1.4 mm).

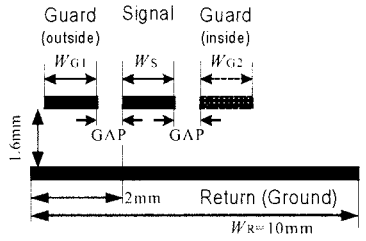

Fig. 5 Cross-section of section BC

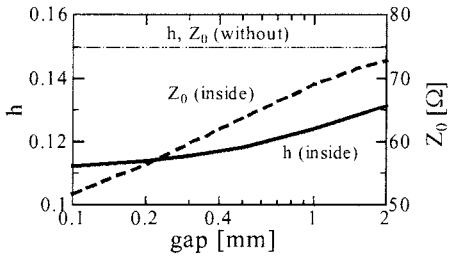

Fig. 6 CDF and characteristic impedance for different widths of the gap between signal and guard traces.

Figure 6 shows the CDF (h) and the characteristic impedance for different widths of the gap between the signal trace and the guard trace in PCB (3). The CDF decreases as the gap narrows. We selected a gap of 0.3 mm, which was the manufacturing limit, for all test PCBs. The characteristic impedance also decreases as the gap narrows. For PCBs (5) and (6), we adjusted the signal trace width to match a characteristic impedance of 75 Ω. The widths of the signal and guard traces and the CDF values are shown in Table 1.

The CDF (h) for section BC was calculated for the transmission line cross-section as shown in Fig. 7. The surrounding conductor is the system ground, which is far from the transmission line. The CDF is given as

$$h = \frac{Q_1}{Q_1 + Q_2 + Q_3}, \quad (5)$$

where Q_1, Q_2, and Q_3 denote the charges on the signal, the return, and the guard conductors, respectively, calculated through two-dimensional static field analysis when these conductors are set to 1V. These charges were calculated using the boundary element method. In this calculation, we ignored the dielectric materials and the conductor thickness.

Table 1 shows that the outside guard structure works better than the inside guard structure, and the

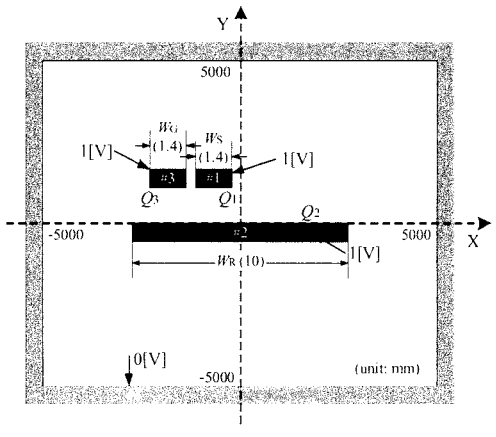

Fig. 7 Analysis model.

Table 1 Dimensions and calculated values for PCBs

Type	W_{G1} [mm]	W_S [mm]	W_{G2} [mm]	Z_0 [Ω]	h_{BC}	ΔE [dB]
(1)	-	1.4-	-	75	0.151	0
(2)	1.4	1.4	-	59	0.095	-4.1
(3)	-	1.4	1.4	59	0.116	-2.3
(4)	1.4	1.4	1.4	50	0.065	-7.4
(5)	1.4	0.7	-	75	0.067	-7.1
(6)	1.4	0.4	1.4	74	0.028	-14.5

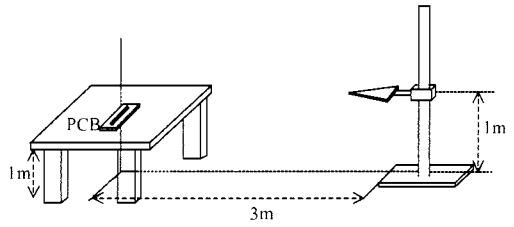

Fig. 8 Measurement setup.

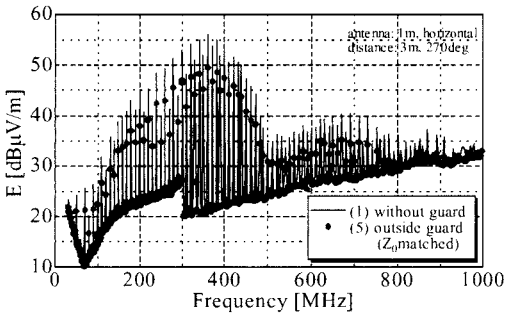

Fig. 9 Comparison of radiated emission/

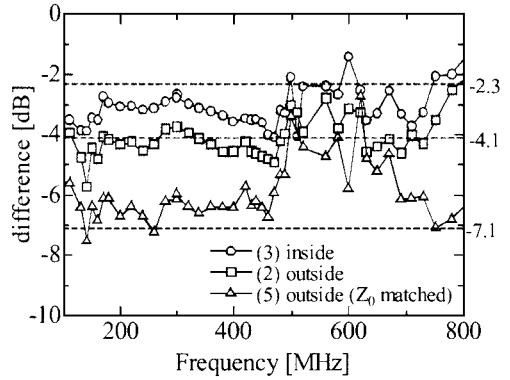

Fig. 10 Suppression of radiated emission.

impedance-matched guard structure is more effective because of the decreased signal trace width. We can calculate these values within 10 seconds per PCB. Therefore, these trials are suitable for practical PCB design.

3.6 Measurement Results

We fabricated samples of the test PCBs listed in Table 1. We measured the radiated emissions from these PCBs in an anechoic chamber as shown in Fig. 8. The PCB was put on a table and the antenna was located 1 m above the metal floor. The radiated emission with a horizontal polarization is shown in Fig. 9. The difference between the radiation from each PCB and that from PCB (1) is shown in Fig. 10. The calculated suppression values are also shown. The decreased suppression above 500 MHz was due to the low emission.

4. Conclusion

Common-mode radiation due to an insufficient ground plane can be explained in terms of differences in line imbalance. We have developed a new calculation procedure based on the imbalance difference model. In this procedure, the radiated emission is separated into three factors: normal mode voltage, the imbalance difference, and the radiation factor of the common-mode antenna. Each factor separately does not require much calculation time, so this calculation method is much faster than the commonly used three-dimensional numerical calculations. Therefore, this calculation method can be applied to practical PCB design. In this paper, we have shown an example of a design procedure based on this calculation method. The evaluated suppression of EMI was confirmed through measurement.

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