# Performance of an Adaptive Array Antenna with a Systolic Array Processor

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## 1. Introduction

Adaptive array antennas generally improve the signal-to-noise ratio in the antenna output by adjusting a set of amplitude and phase weights so as to produce a far-field pattern that optimizes the reception of a desired signal. Therefore, much work has been done on development and analysis of weight control algorithms [1].

Recently, for the purpose of developing an adaptive array antenna which has rapid convergence and high cancellation performance, a new architecture for an adaptive array antenna was proposed which applies direct solution or open loop techniques to adaptive antenna processing [2,3]. The basic function is formulated as a recursive least squares minimization operation under the directionally constraint condition [4]. This algorithm can be implemented using a pipelined architecture in the form of a triangular systolic array processor (SAP) [5,6]. This architecture has many desirable features for very large scale integration (VLSI) system design [7].

In this paper, we describe interference and multipath suppression performance of the adaptive array antenna with SAP (SAP-AA) by using computer simulations.

# 2. Configuration of the SAP-AA

A generic configuration for the SAP-AA is illustrated in Fig.1. It was proposed in the literature [2,3]. This system requires the knowledge on the direction of the desired signal. A chosen look direction defines the corresponding coefficients  $c_i(i = 1, 2, ..., N - 1)$ . The function of the SAP-AA is to minimize the combined array output |e(t)| under the linear beam constraint condition. This constraint ensures that the gain of the antenna array maintains a constant value in the desired signal direction of arrival. A combined array output can be therefore the desired signal. A signal processor is implemented in a very efficient pipelined manner using a triangular SAP. Many cells which have the same structure and function are included and regularly located in the SAP. The pipelined computations take place along all cells and result in very high computational throughput.

## 3. Interference and multipath suppression performance

In this section, we show computer simulation results of the SAP-AA in several signal environments. Fig.3 shows a frequency spectrum in case two narrow band signals, a desired signal and an interference, are incident on the array. A linear array is used with 3-antenna elements and half-wavelength element spacing. The antenna elements are assumed to be omnidirectional and of comparable. Moreover, the desired signal and the interference arrive from the broadside and 10° apart from it, respectively. Each spectrum shown in Fig.3 corresponds to the output of the third antenna element (Fig.(a)) and the array output after the transient response, respectively. In these figures, a horizontal axis represents frequency normalized by a 3-dB bandwidth of a third-order Butterworth filter by which thermal noise is band-limited and a vertical axis represents the value normalized by the thermal noise power. These figures imply that a good interference cancellation is obtained, maintaining the level at the desired signal constant.

Next, we describe the multipath suppression performance in case two multipath signals, a desired signal and an undesired signal, are incident on the array. The undesired signal is a delayed and phase-shifted version of the desired signal. The signal directions of arrival are the same as those in Fig.3. The modulation method is quadriphase-shift keying (QPSK) with a symbol length T. Namely, we have a bit rate of 2/T. We assume that the signals and thermal noise are band-limited by a third-order Butterworth filter with a 3-dB bandwidth of 2/T. Fig.4 shows envelopes of inphase signal components. In the simulation, the delay and phase shift of the undesired signal are determined as 1.0T and 10.33° compared with the desired signal. In these figures, a horizontal axis represents the time normalized by T and a vertical axis represents amplitude. The desired signal incident on the third antenna element is shown in Fig.4(a). Fig.4(b) shows the output of the third antenna element which includes the desired signal, the undesired signal and thermal noise. Fig.4(c) shows the array output. In Fig.(b) and (c), the desired signal is also displayed by a broken line. While the antenna output in Fig.(b) is much different from the desired signal, the array output in Fig.(c) is almost the same as the desired signal for the time  $\geq 2$  or 3 according to the effective suppression for the undesired signal.

Then, we show the simulation results in case the delay of the undesired signal is 0.5T. While the array output in Fig.5(c) is much distorted, it is helpful in order to test signs correctly for the time  $\geq 9$ .

From these results, the SAP-AA is said to be effective for the multipath suppression.

#### 4. Conclusion

Interference and multipath suppression performance of the SAP-AA was shown by computer simulations. It is expected from these results that the SAP-AA is effective for the interference and multipath suppression.

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#### References

- R. A. Monzingo and T. W. Miller, Introduction to Adaptive Array, New York: Wiley-Interscience, 1980.
- [2] C. R. Ward, P. J. Hargrave and J. G. McWhirter, "A Novel Algorithm and Architecture for Adaptive Digital Beamforming," IEEE Trans. Antennas Propagat., Vol.AP-34, No.3, Mar. 1986.
- [3] J. V. McCanny and J. G. McWhirter, "Some Systric Array Developments in the United Kingdom," IEEE Computer, Vol.20, No.7, pp.51-63, Jul. 1987.
- [4] J. G. McWhirter, "Systolic Array for Recursive Least- Squares Minimization," Electronics Letters, Vol.19, No.18, Sep. 1983.
- [5] L.S.Haynes (eds.): IEEE Computer, Special Issue on Highly Parallel Computing, Vol.15, No.1, Jan. 1982.
- [6] J. A. B. Fortes, and W. Wah (eds.): IEEE Computer, Special Issue on Systric Arrays, Vol.20, No.7, Jul. 1987.
- [7] H. T. Kung and C. L. Leiserson, "Systric Arrays (for VLSI)" in C. A. Mead and L. A. Conway, "Introduction to VLSI system," Addison Wesley, 1980.



Input signal-to-noise ratio is 20dB, Input Interference-to-noise ratio is 30dB, and the desired signal and interference directions of arrival are 0° and 10°, respectively.



Fig.3 Multipath cancellation performance (1).

Input desired signal-to-noise ratio as same as input undesired signal-to-noise ratio is 20dB. The delay of the undesired signal compared with the desired signal is 1.0T.



<sup>(</sup>c) array output (solid line) and desired signal (broken line).

Fig.4 Multipath cancellation performance (2).

Input desired signal-to-noise ratio as same as input undesired signal-to-noise ratio is 20dB. The delay of the undesired signal compared with the desired signal is 0.5T.