Improved Implement of S-Parameter for the FDTD Method

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1 Introduction

In the design of antennas or circuits with complex structure, it is necessary to analyze the problems including mutual coupling between elements and radiations effect. Finite Difference Time-Domain (FDTD) method is a well-known technique to solve these problems. However, it is difficult to make a simulation model for real structure of circuits. An accurate equivalent circuit model is widely used to overcome these difficulties[1]-[3]. The equivalent circuit should be selected for each element and it is cumbersome for circuit design. Therefore, it is very attractive method to involve the circuit element expressed as S-parameter into circuit simulators or electromagnetic (EM) simulators. In recent years, it has been proposed to use this method for EM analysis implementing element expressed as S-parameter[4],[5]. However, a further improvement in the modeling is necessary to achieve high accuracy. In this paper, we clarify the problems of implementing S-parameter to the FDTD analysis using a simple linear circuit, which are not presented in the conventional method [4]. Then we present analytical techniques to improve the accuracy for the FDTD calculation and verify them by the measurement.

Important factors discussed in this paper to make simulation model are as follows, (a) how to use the resistor termination in the via model in order to absorb an incident wave at the part of S-parameter, (b) the difference between Faraday's laws and the method computed from the electric field in the calculation of the observing voltage at S-parameter part, and (c) how many vias are appropriate to express the width of microstrip line (MSL). These three factors will be discussed in detail in this paper.

2 Implementation of S-parameter for the FDTD method

In the beginning, we explain how to implement of S-parameters to the FDTD method. S-parameter $S(t)$ in the time-domain is computed by inverse Fourier transform of S-parameter $S(f)$ in the frequency-domain, where it is converted by the discrete time step Δt in the FDTD analysis. The reflection voltage V_{11} at a port 1 and the transmission voltage V_{21} from the port 1 to port 2 are computed by convolution integral of an incident wave V_{1in} at the port 1 and $S(t)$ as follows.

$$V_{i1}[n] = S_{i1}[n] * V_{1in}[n] \qquad (i = 1, 2) \tag{1}$$

Here, V_{1in} is approximated by the observing voltage V_{1view}, V_{11}, and V_{12} computed before one time step at port 1 as follows.

$$V_{1in}[n] \simeq V_{1view}[n-1] - V_{11}[n-1] - V_{12}[n-1] \tag{2}$$

V_{12} and V_{22} are calculated in the same procedure by adding the incident wave to port 2, the voltage source are excited to each port. A 50Ω resistor termination is applied to the input port for absorbing the incident wave as shown in Fig. 1.

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In this method, 50Ω resistor termination does not absorb the incident wave completely. Figure 2 shows a sample circuit of a chip capacitor at a gap of 50Ω MSL. A small reflection pulse around 1000 steps as shown in Fig. 3 causes errors in the calculation of S-parameter. A conventional implementation method by lumped element circuit is given by

$$E_Z^n = \frac{1 - \frac{\Delta t \Delta z}{2R\epsilon\Delta x \Delta y}}{1 + \frac{\Delta t \Delta z}{2R\epsilon\Delta x \Delta y}} E_Z^{n-1} + \frac{\frac{\Delta t}{\epsilon}}{1 + \frac{\Delta t \Delta z}{2R\epsilon\Delta x \Delta y}} (\nabla \times H^{n-\frac{1}{2}}). \tag{3}$$

In this paper, we use a simple expression given in eq.(4) to improve absorbing characteristics.

$$E_Z = \frac{RI}{\Delta z} \tag{4}$$

The level of S_{11} is improved by 3 dB in the frequency range of 4 GHz up, which shows the effectiveness of the proposed method. An *ideal* curve in Fig. 4 is given by assuming the incident wave absorbed completely.

Next we discuss the computation method to obtain V_{1view}. The voltage is computed from the electric field expressed by eq.(5) in this paper, whereas the conventional method by Faraday's law is expressed by eq.(6) as follows.

$$V_{1view} = E_Z \Delta z \tag{5}$$

$$\begin{gathered} V_{1view} = -L_0 \frac{dI_{1view}}{dt} - V \\ L_0 = 1 / \sum_{i=1}^{4} \frac{1}{L_i} \quad , \quad V = L_0 \sum_{i=1}^{4} \frac{V_i}{L_i} \end{gathered} \tag{6}$$

The current is obtained by applying Faraday's law along contour from P_1 through P_4 as shown in Fig. 5. V_{1view} is derived from currents I_{1view} calculated by these contour and space inductance in FDTD. Figure 6 shows the difference according to this implementation method. A simple V_{1view} expression by eq.(5) gives a little bit deep S_{11} at 4 GHz, which improves the over all characteristics.

At last, we examine the number of via to express the width of MSL as shown in Fig. 7. As shown in Fig. 8, one via model gives good S_{11} characteristic compared with a use of several vias.

3 Calculation and experiment result of LPF using S-parameter

In order to confirm validity of our improve method, S_{21} characteristics are calculated using a simple low pass filter (LPF). Table 1 shows the FDTD analysis parameters in this paper. LPF is the structure using the chip inductor expressed as the S-parameter in MSL as shown in Fig. 9. To evaluate this implementation, we compared the measurement result of LPF with the simulation result of FDTD implemented S-parameter and that of circuit simulator in commercially use as shown in Fig. 10. In addition, proposed method gives good S_{21} characteristic compared with the conventional method in S-parameter implementation. Especially in high frequency more than 6 GHz, proposed method is good agreement with the measurement. Moreover, it is confirmed that the simulation result by the proposed FDTD implementation agrees well with the measurement result compared with result of circuit simulator, because mutual coupling between elements is included by S-parameter implementation.

4 Conclusion

The analysis method implemented S-parameter to the FDTD was presented to increase the accuracy of simulation. The effectiveness of this implementation method was confirmed by the measurement result.

References

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Table 1: FDTD analysis parameter

Analytic Region	175×60×39cell
Cell size	$\Delta x = 0.5mm$, $\Delta y = 0.55mm$, $\Delta z = 0.533mm$
Iteration	25,000 time steps
Discrete time	$\Delta t = 0.8ps$
Incident wave	Gaussian pulse
ABC	PML 5 layer

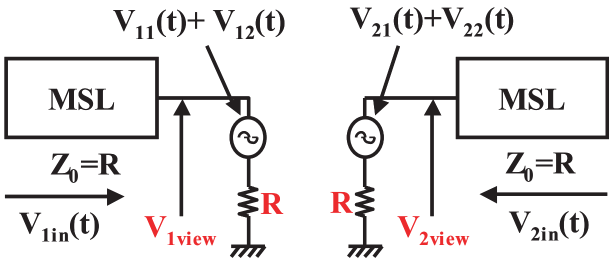

Figure 1: Equivalent circuit of two port circuit and the implementation of S-parameter

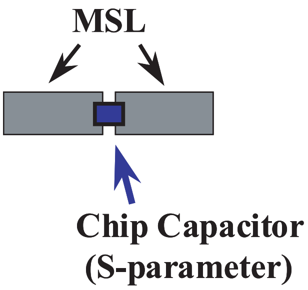

Figure 2: Analytic model of series chip capacitor

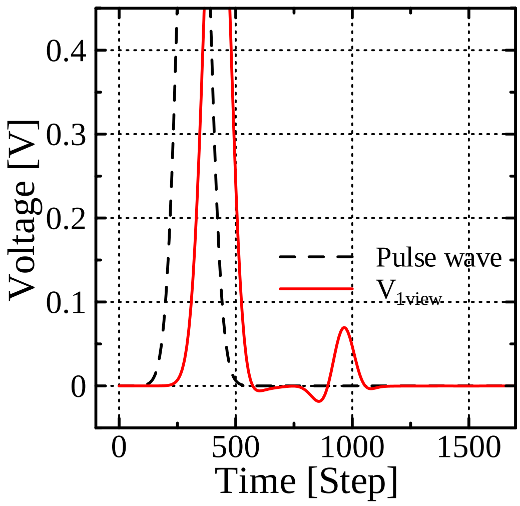

Figure 3: Observation voltage (V1view) at port 1

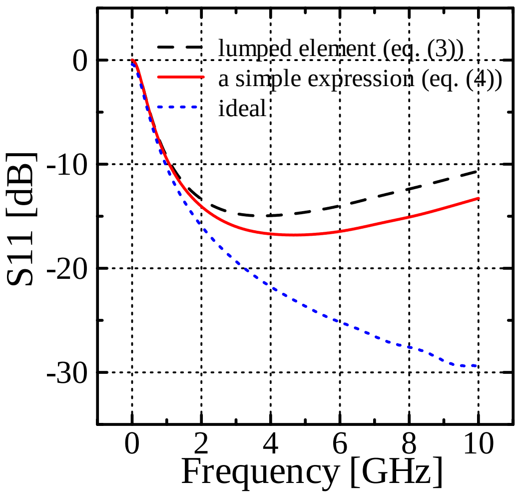

Figure 4: S11 characteristics of three implementation methods for resistor termination

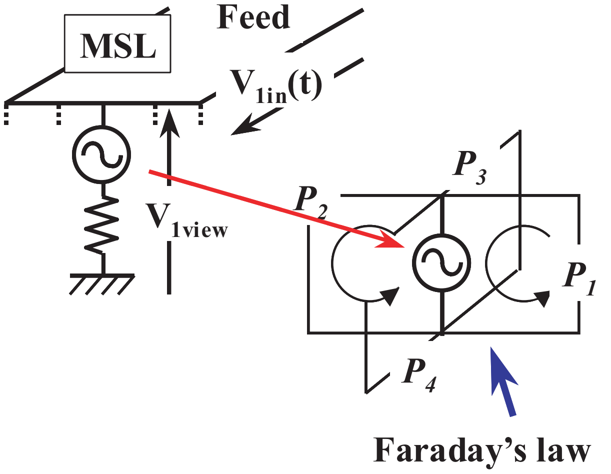

Figure 5: Analytic model of observation voltage by applying Faraday's law

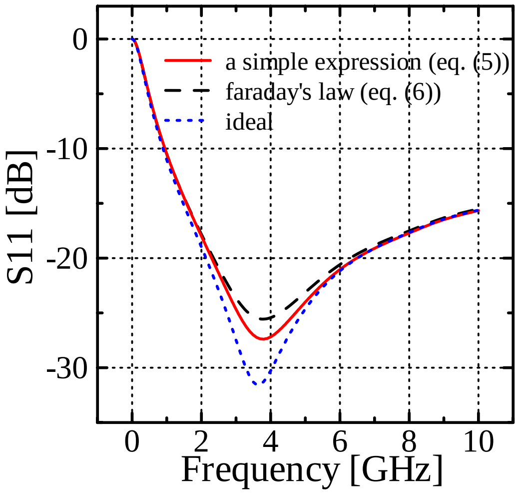

Figure 6: S11 characteristics of three analytic methods for observation voltage

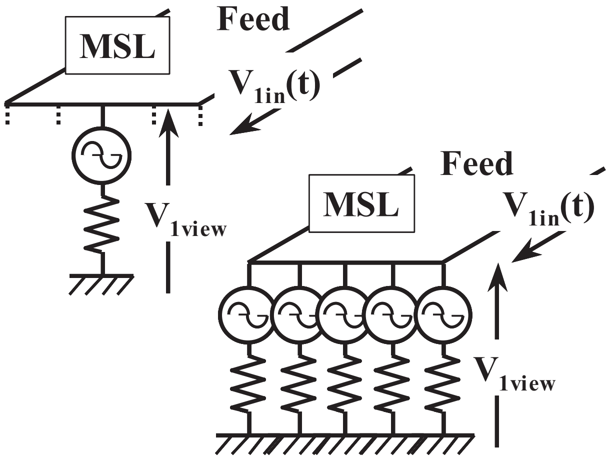

Figure 7: Implementation of via for voltage source

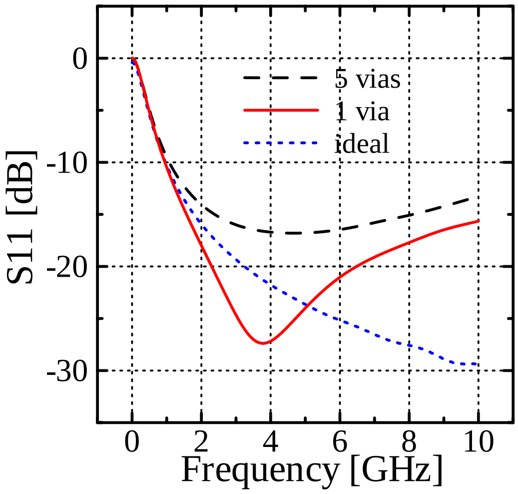

Figure 8: S11 characteristics of three implementation methods for vias

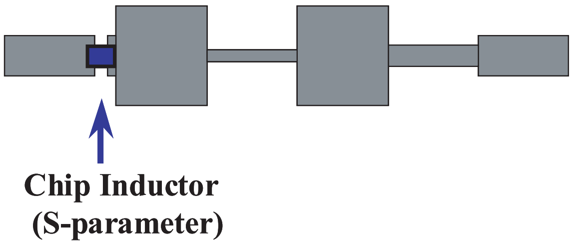

Figure 9: Layout of LPF

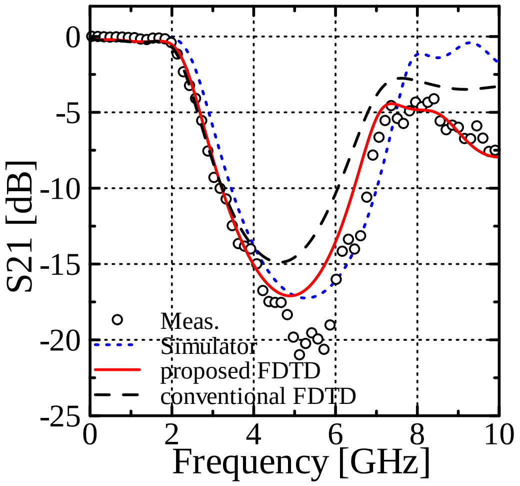

Figure 10: S21 characteristics of calculated and measured results of LPF