

60 GHz On-Chip Patch Antenna Integrated in a 0.18- μm CMOS Technology

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1. Introduction

Millimeter-wave CMOS RF circuits have been received substantial attention, motivated by the advance of CMOS process [1]. In the millimetre-wave band, the connection, such as wire bonding or flip chip bonding, between the RF circuit and off-chip antenna is not easy task because of the radiation loss and/or adding parasitic components. To overcome the problem, on-chip antennas, which do not suffer from the problem of connection, have been studied by many researchers [2][3]. Accurate and appropriate modelling in simulation is very important to obtain agreement with measurement.

In this paper, a 60 GHz on-chip patch antenna integrated in a 0.18- μm CMOS technology is investigated by simulation and measurement. Very good agreement for frequency characteristic of reflection coefficient is observed between simulation and measurement, which enables further investigation by simulation.

2. On-Chip Patch Antenna

The configuration of an on-chip patch antenna is shown in Fig. 1. Antenna dimensions are shown in Fig. 1 (a). Chip photo is shown in Fig. 1 (b). The patch antenna is fed by a nearly 50 Ω microstrip line (MSL). In the measurement, a 100 μm pitch GSG pad is used to attach with a GSG probe. The configuration of the GSG pad and MSL [4] is shown in Fig. 1 (c). The bottom metal layer is used for the ground plane of the MSL and the patch antenna. The top metal layer is used for the signal line of the MSL and the patch. The height h between the bottom metal to the top metal is about 5 to 10 μm , and metal thickness is about 0.5 μm to 1 μm in commercial CMOS technology. The metal of the metal is aluminium and the insulator between the metal is SiO₂. There is a line with 625 μm -length and 30 μm -width between the MSL and the patch antenna for impedance matching.

3. Results

The frequency characteristic of reflection coefficient is shown in Fig. 2. The reference plane is shown in Fig. 1 (b). In the measurement, the influence of the pad is removed by de-embedding technique using thru and line patterns [5][6]. The reflection is about -10 dB at design frequency 62.5GHz. The simulated result agrees very well with the measured one both in amplitude and phase. The finite element method (FEM) based commercial software Ansys HFSS ver.11 is used in this paper for the simulation.

The simulation model is shown in Fig. 3 (a). The excitation is modelled by the lumped port with 50 Ω impedance at the edge of the MSL. Conductor loss of aluminium is considered while dielectric loss is neglected in the simulation. Calculated radiation pattern is shown in Fig. 3 (b). Calculated peak gain and radiation efficiency were -14.5 dBi and 1.0 %, respectively. Therefore, it is found that the conductor loss is dominant in degradation of radiation efficiency in the on-chip patch antenna because the height h is very thin ($\sim 2/1000$ wavelength).

Figure 4 shows calculated radiation efficiency as a function of MSL height h . It is found that radiation efficiency becomes large enough when h is larger than $100\mu\text{m}$ ($\sim 2/100$ wavelength).

4. Conclusion

A 60 GHz on-chip patch antenna integrated in a $0.18\text{-}\mu\text{m}$ CMOS technology is evaluated by simulation and measurement. The agreement between measurement and simulation was very good in the frequency characteristic of reflection coefficient. The calculated peak gain and radiation efficiency were -14.5 dBi and 1.0% , respectively. It is found that the conductor loss is dominant in degradation of radiation efficiency in the on-chip patch antenna when the height is very thin ($\sim 2/1000$ wavelength). The radiation efficiency becomes large enough when height is larger than $100\mu\text{m}$ ($\sim 2/100$ wavelength). Experimental evaluation of radiation pattern and radiation efficiency is a future task. Improvement of radiation efficiency is also remaining as a future study.

Acknowledgments

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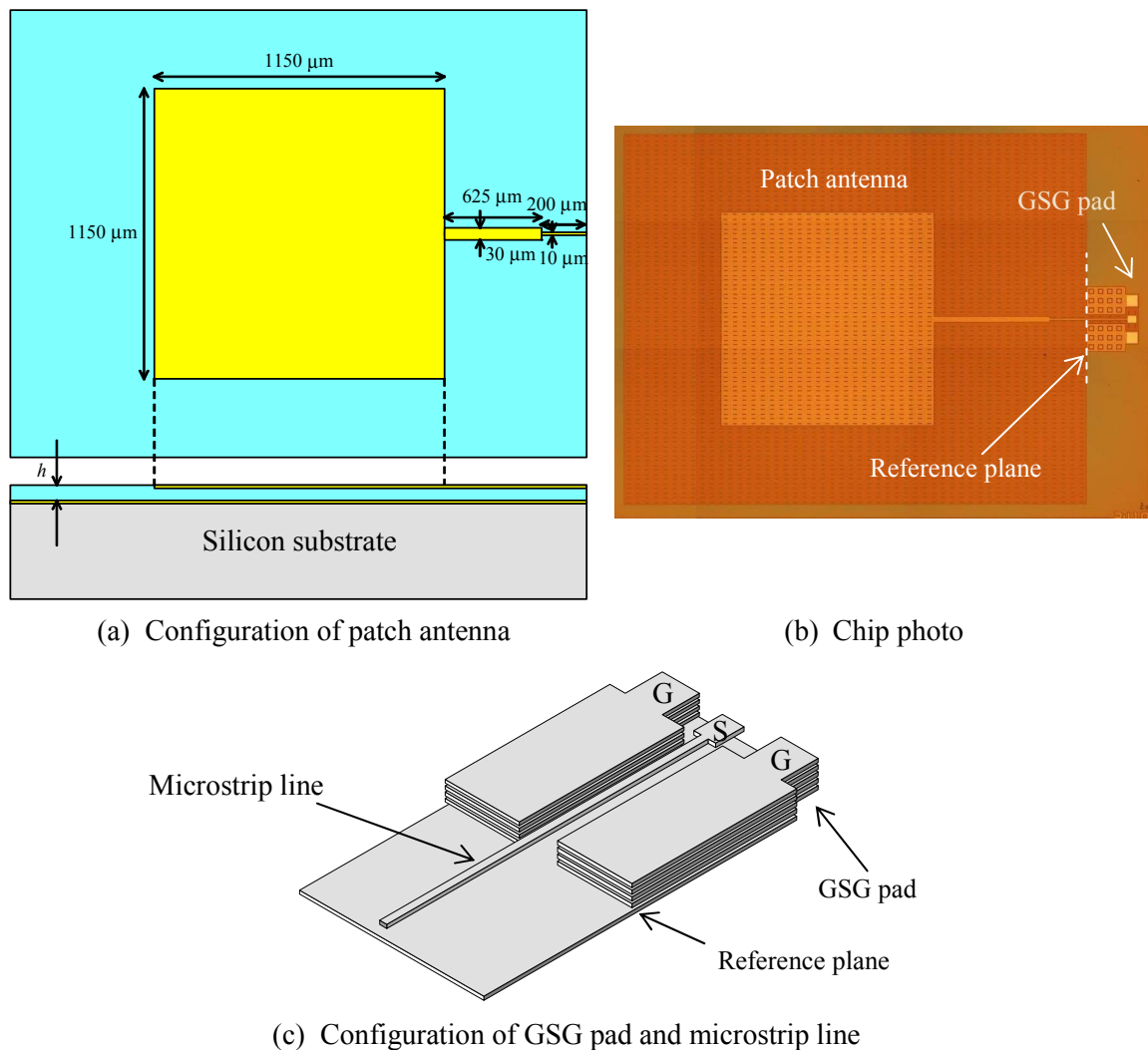


Figure 1: On-chip patch antenna

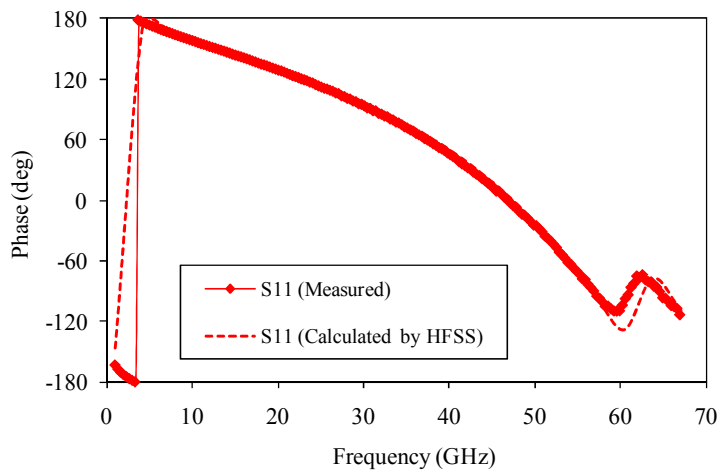
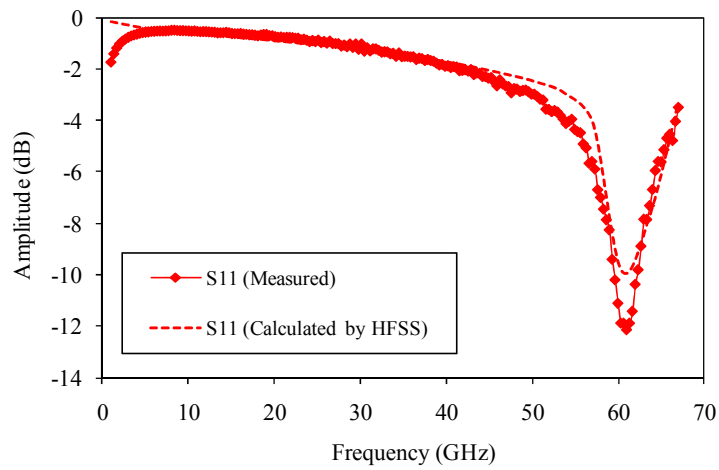
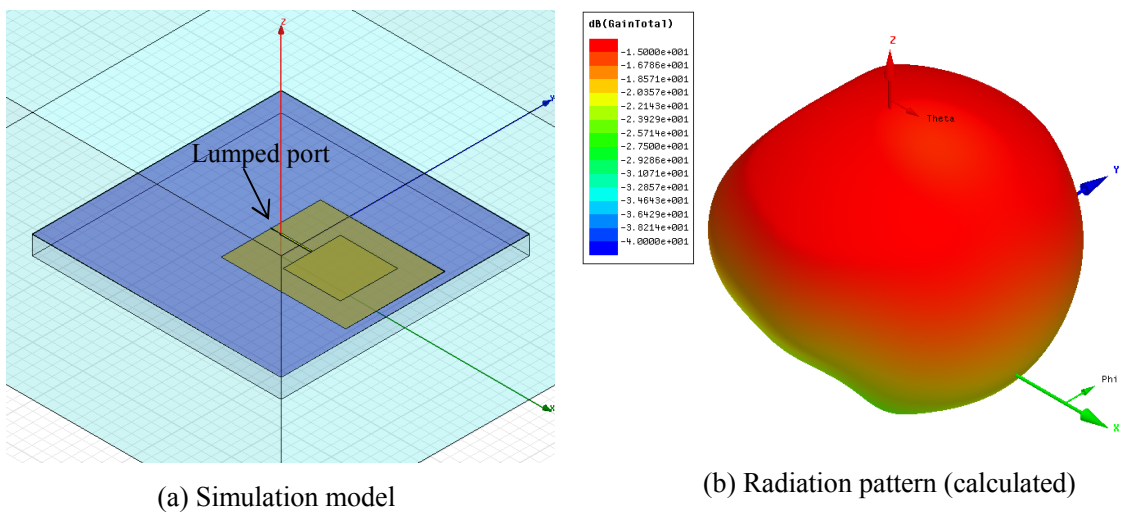


Figure 2: Frequency characteristic of reflection coefficient



(a) Simulation model

(b) Radiation pattern (calculated)

Figure 3: Simulation model and radiation pattern

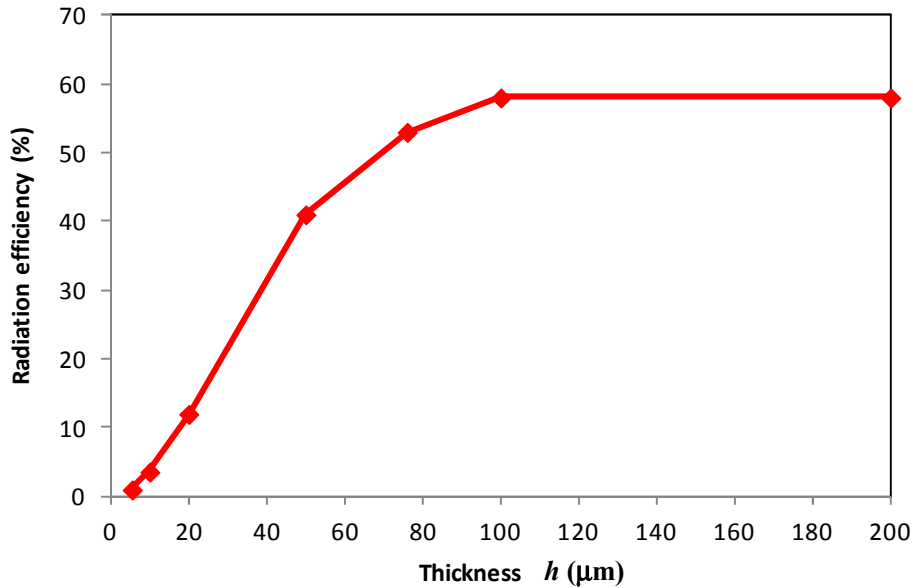


Figure 4: Radiation efficiency as a function of MSL height (calculated)

References

- [1] C.H. Doan, S. Emami, D.A. Sobel, A.M. Niknejad, and R.W. Brodersen, "Design considerations for 60 GHz CMOS radios," *IEEE Communications Magazine*, Vol.42, No.12, pp.132-140, December 2004.
- [2] K. Payandehjoo and R. Abhari, "A novel technique for coupling reduction between closely spaced on-chip antennas for millimeter-wave applications," *Proc. of IEEE Antennas and Propagation Society International Symposium*, July 2010.
- [3] K.-K. Huang and D.D. Wentzloff, "A 60 GHz Antenna-Referenced Frequency-Locked Loop in 0.13 μm CMOS for Wireless Sensor Networks," *IEEE Journal of Solid-State Circuits*, vol.46, no.12, pp.2956-2965, Dec. 2011.
- [4] Y. ONO, T. HIRANO, K. OKADA, J. HIROKAWA, M. ANDO, "Eigenmode Analysis of Propagation Constant for a Microstrip Line with Dummy Fills on a Si CMOS Substrate," *IEICE Trans. Electron.*, Vol.E94-C No.6, pp.1008-1015, June 2011.
- [5] T. Hirano, K. Okada, J. Hirokawa, and M. Ando, "Thru-Line (TL) Calibration Technique for On-Wafer Measurement," *Proceedings of International Symposium on Antennas and Propagation (ISAP)*, Paper ID: 104, November 2010.
- [6] T. Hirano, K. Okada, J. Hirokawa, and M. Ando, "Accuracy Investigation of De-embedding Techniques Based on Electromagnetic Simulation for On-wafer RF Measurements," in "Numerical Simulations", *InTech Open Access Book*, ISBN 979-953-307-821-1, August 2012. (to be published)