Effect of Cosine Rolloff Filter on Low-IF Multi-Channel Receiver in Digital Communication System

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Abstract

Software defined radio (SDR) technology has been attracted due to its flexibility and efficient performance in mobile communication. This paper presents an efficient scheme of multichannel low-IF receiver that improves digital communication quality in the sense of BER performance and computational cost. Simply adding cosine rolloff filters to the conventional multichannel receiver, the proposed receiver achieves much higher accuracy, smaller circuit and shorter computation time to process than the conventional one.

1. INTRODUCTION

Software defined radio (SDR) technology has been attracted due to its flexibility and efficient performance in mobile communication. One of the significant issues in SDR technology would be the receiver architecture that often requires high-speed A/D converters as well as high-speed digital signal processor. Receivers with direct conversion technique [1] may become a solution for such a problem, however the performance of the direct conversion receiver is limited due to the effect of DC offset. The alternative receiver may be Low-IF receiver which is more suitable for multichannel signal reception [1], [2], used in wireless local area network for example. It does not require any high-speed A/D converter, but is seriously interfered from adjacent frequency channels especially in severe propagation environments.

To dissolve those problems, a multichannel receiver using complex analog-digital signal processing has been already proposed [3], [4]. Its complex signal processing enables to independently assign plus/minus frequency bands to multichannel signals and realizes efficient multichannel signal processing. But its performance becomes worse when there exist large interferences or when the signals are multivalued modulated (means in both amplitude and phase) such as 16QAM. Indeed its circuit scale becomes large due to two independent processes which correspond to the desired and interference signals.

In this paper, we propose an efficient scheme of multichannel low-IF receiver by simply adding cosine rolloff filters (CRFs) between A/D converters and LMS optimizer in the conventional receiver [3]. We will show that the CRFs work effectively through some computer simulation, and mention that LMS optimizer is no longer needed in the proposed scheme. Then the proposed receiver can be implemented without the interference processing scheme while preserving high accuracy, that enables to reduce circuit and computational costs.

This paper is organized as follows: Section 2 explains the system model of the conventional and proposed ones. Section 3 shows the results of the computer simulations to evaluate the effect of the proposed receiver. Finally, in Section 4 we make some concluding remarks.

2. SYSTEM MODEL

A. Conventional Model

The circuit construction of the conventional receiver in [3] is shown in Fig. 1. The downconverted signal $r(t)$ (after RF-Mixer & Amplifier) is expressed as

$$r(t) = d(t)\exp(j\omega_I t) + I(t)\exp(-j\omega_I t) + n(t), \qquad (1)$$

where $d(t), I(t), \omega_I, -\omega_I$ and $n(t)$ denote desired signal, interference signal in the adjacent channel, the intermediate frequency of desired signal, that of interference signal, and noise signal, respectively.

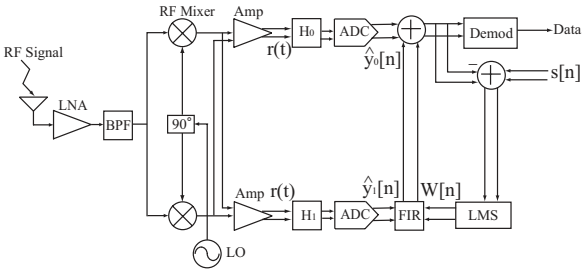


Fig. 1: The conventional multichannel receiver in [3].

The analog filters $\boldsymbol{H}_0$ and $\boldsymbol{H}_1$ respectively extract the desired and interference signals from the downconverted signal

$r(t)$. Then the outputs of the analog filters $y_m(t)$ are digitized as

$$\hat{y}_m[n] \quad = \quad \mathrm{adc}\{y_m((n-1)T_s)\}, \quad m = 0, 1, \qquad (2)$$

where $\hat{y}_m[n]$ is the output of A/D converters and also the input to the LMS process. The LMS processor is employed to further suppress the interference that still exists in the desired signal $\hat{y}_0[n]$. That becomes important when the interference has a large power and cannot be well suppressed by the analog filter $\boldsymbol{H}_0$.

B. Proposed Model

The proposed receiver model is depicted in Fig. 2. The only difference between the receivers in Figs. 2 and 1 is whether there exist CRFs $\boldsymbol{G}_0$ and $\boldsymbol{G}_1$ between A/D converters and LMS processors. The aim of adding CRFs is same to the LMS processor in [3], to further suppress the interference that still exists in the output signal of $\boldsymbol{H}_0$.

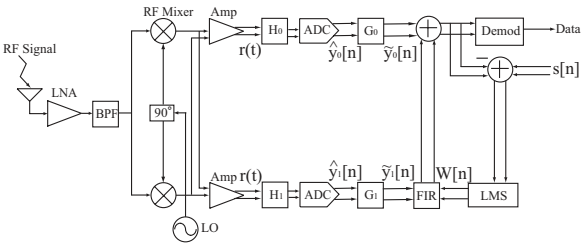


Fig. 2: Model of the proposed receiver.

In this case, the input to the LMS processor $\tilde{y}_m[n]$ is given by the discrete convolution of the impulse response of CRFs $g_m[n]$ and the output of the analog filters $\hat{y}_m[n]$ in (2), i.e.,

$$\tilde{y}_m[n] \quad = \quad \sum_{k=0}^{L-1} g_m[k]\hat{y}_m[n-k], \quad m = 0, 1, \qquad (3)$$

where L is the order of CRFs. The rest processes of the receiver are same to those described in the previous subsection.

C. Proposed Model (Further Simplified)

As we will show in the next section, CRFs can efficiently suppress the undesired components and consequently we can achieve high accuracy in the sense of BER performance without the LMS processor. Therefore the proposed receiver is further simplified by removing the LMS processor and also the interference signal processing module. Resulting circuit construction is as shown in Fig. 3, requires less than a half circuit cost in comparison with Fig. 2 by serial processing. We will see that this low-cost circuit can achieve good performance in the next section.

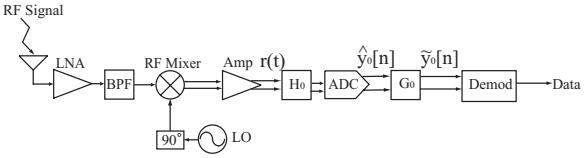


Fig. 3: Simplified model of the proposed receiver.

3. SIMULATION

The proposed receivers are evaluated through computer simulation whose specifications are summarized in Table 1. We assume the case that the frequency bands for the desired and the interference signals are next to each other, and demonstrate to suppress the interference signal. Also note that we employed the same complex analog filter with [3].

TABLE 1: SPECIFICATIONS OF SIMULATION.

Modulation type	Desired: QPSK / 16QAM Interference: QPSK / 16QAM
Frequency range	Desired: [0MHz, 10MHz] Interference: [−10MHz, 0MHz]
Sampling frequency	20MHz
# of analog filters	4 or 5
FIR filter order	31
Step size	10^{-4}
# of bits	100,000
Training period	1,000
CRF order L	15
Rolloff rate	0.5

A. Impulse Responses of CRFs

The impulse responses and the amplitude characteristics of the designed CRFs with $L = 15$ are shown in Table 2 and Fig. 4(b), respectively. Note that the following equations hold for $n = 8, 9, \ldots, 14$.

$$g[n] \quad = \quad g[L-n-1], \qquad (4)$$

$$g_m[n] \quad = \quad -g_m[L-n-1], \quad m = 0, 1. \qquad (5)$$

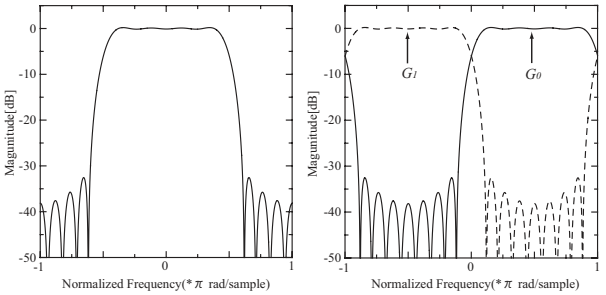
We first design the CRF with the real impulse response $g[n]$ whose amplitude is as in Fig. 4(a), and then the amplitude is $\pi/2$-shifted (solid line in Fig. 4(b)) and also $-\pi/2$-shifted (broken line in Fig. 4(b)) to extract only the desired and interference signals, respectively. The shifted versions have only one complex (pure imaginary) value at the center of their impulse responses, and all the others are real values as seen in Table 2. From this fact, we can confirm that the complex digital filtering does not make the computational cost larger.

B. BER Characteristics

Figure 5 shows the BER characteristics for QPSK signals when the number of analog filter stages is 5, which is same to the case in [3]; (a) when changing the resolution of the A/D converters while fixing SIR to -40[dB] and SNR to 0[dB], and (b) when changing SIR while fixing the A/D converter resolution to 8[bit] and SNR to 0[dB]. Note that the broken

TABLE 2: IMPULSE RESPONSES OF CRFS WHEN $L = 15$.

n	$g[n]$	$g_0[n]$	$g_1[n]$
0	-0.0204	-0.0204	0.0204
1	0	0	0
2	0.0433	0.0433	0.0433
3	0	0	0
4	-0.0928	-0.0928	-0.0928
5	0	0	0
6	0.3137	-0.3137	-0.3137
7	0.5	$-0.5j$	$0.5j$



(a) Before shifting (b) After shifting

Fig. 4: Amplitude characteristics of the designed CRFs.

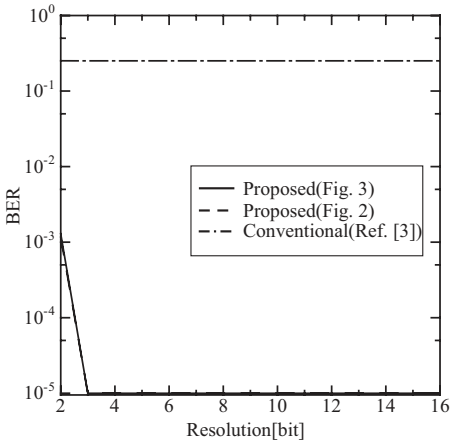
line by the proposed receiver in Fig. 2 completely overlaps the solid line. From Fig. 5, we see that the proposed receivers could greatly improve the BER characteristics, even when we employ the simplified receiver developed in subsection 3.3. We also see that at least 4[bits] resolution in A/D conversion is required for good BER performance.

Figure 6 shows the BER characteristics when the number of analog filter stages is 4; (a) when changing the A/D converter resolution and (b) when changing SIR. Similarly to the behavior in Figure 5, the BER characteristics by the proposed receivers could enhance BER performance in comparison with the conventional receiver especially in severe environments like lower SIR or shorter resolution of A/D converter. From Fig. 6, the proposed receiver can achieve enough high accuracy with only 4 analog filters, that leads to smaller analog circuit cost.

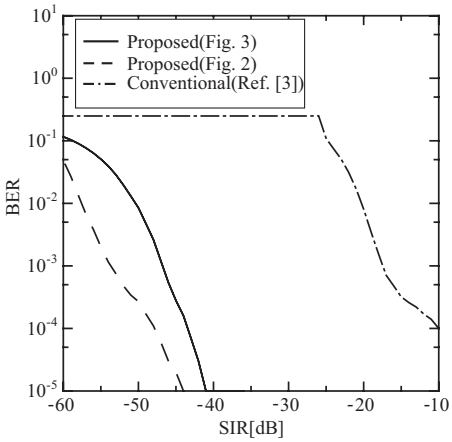
Also Figure 7 shows the BER characteristics for 16QAM signals when the number of analog filter stages is 4; (a) when changing the resolution of the A/D converters while fixing SIR to -20[dB] and SNR to 0[dB], and (b) when changing SIR while fixing the resolution of the A/D converters to 8[bit] and SNR to 0[dB]. Similarly to the cases of QPSK signals, the BER characteristics by the proposed receiver is very much improved in comparison with the conventional scheme. We found from Fig. 7 that the proposed scheme was very efficient, even when the multivalued modulation such as 16QAM is employed.

C. Computational Cost

Computational cost is also compared. All the simulations are done with MATLAB R14, and the specifications of the computer is Windows XP SP2, CPU Pentium IV 3.0GHz, and Memory 1GB. Table 3 compares the computational costs of processing 100,000 symbols. Computation time for LMS is to process the first 1,000 symbols as training symbols in 100,000 symbols. According to the computation time in Table 3, the receiver shown in Fig. 3 requires much shorter time in comparison with the other two receivers.



(a) SIR=-40[dB], SNR=0[dB], changing /AD resolution.



(b) A/D resolution=8[bit], SNR=0[dB], changing SIR.

Fig. 5: BER characteristics for QPSK signals (5 stages of analog filters). Note that the broken line in (a) completely overlaps to the solid line.

TABLE 3: COMPARISON OF COMPUTATIONAL COSTS

	CRF	LMS	Demod.	Total (Ratio)
Fig.1(Ref.[3])	-	4.37	0.05	4.42 (49.1)
Fig.2	0.04	4.37	0.05	4.46 (49.6)
Fig.3	0.04	-	0.05	0.09 (1)

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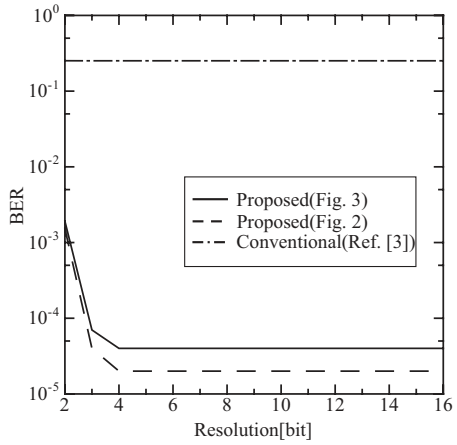
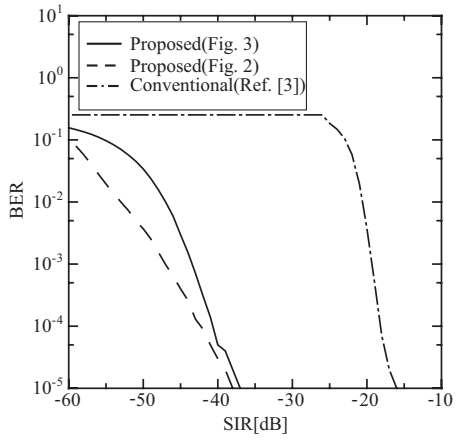
4. CONCLUDING REMARKS

In this paper, we proposed an efficient scheme of multichannel low-IF receiver by simply adding CRFs to the conventional multichannel receiver module, and the proposed receiver could achieve much more accurate quality than the conventional receiver at smaller circuit and computational costs. The proposed

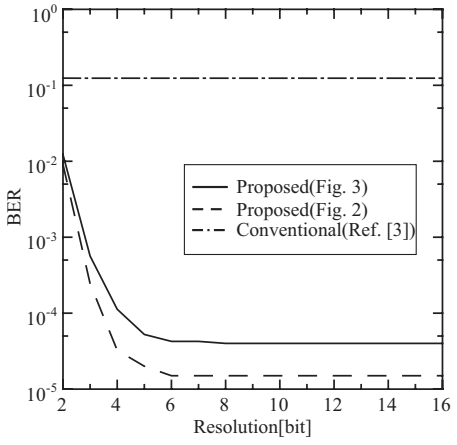


(a) SIR=−40[dB], SNR=0[dB], changing A/D resolution.

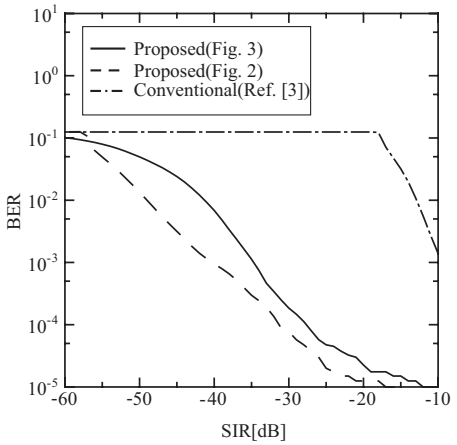


(b) A/D resolution=8[bit], SNR=0[dB], changing SIR.

Fig. 6: BER characteristics for QPSK signals (4 stages of analog filters).



(a) SIR=−20[dB], SNR=0[dB], changing A/D resolution.



(b) A/D resolution=8[bit], SNR=0[dB], changing SIR.

Fig. 7: BER characteristics for 16QAM signals (4 stages of analog filters).

circuit might be only a slight modification from the conventional one, but can greatly enhance the accuracy of digital communication and can reduce both the analog and digital circuit costs by employing desired-only serial processing and smaller number of analog filters.

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