4×4 MIMO Prototype System and Measurement of Indoor Environment

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1. Introduction

Multiple-Input Multiple-Output (MIMO) wireless systems are extensively studied as a technique that increases the communication capacity [1] [2]. The communication capacity depends on the propagation condition and the antenna configuration, etc. Therefore, the studies based on real environment are important. Some 2×2 MIMO system are developed in some research laboratories [3], and we developed a 4×4 MIMO prototype system constructed with a 4-channel transmitter and receiver, Digital-Analog (D/A) and Analog-Digital (A/D) converters. The carrier frequency of transmitter and receiver is tunable. Field Programmable Gate Arrays (FPGAs) and CPU are installed the converters, and both the real-time sequential processing and off-line processing is possible in the system. This system is a general purpose system and used for evaluation of algorithm or hardware in various conditions. In this paper, we introduce the system and show results of basic measurement in an indoor environment.

2. 4×4 MIMO Prototype System

Table 1 shows the specification of the 4×4 MIMO Prototype System. The construction and general view of the system is shown in Fig.1. The system consists of antennas, a DBF transmitter and a DBF receiver, A/D and D/A converters, FPGAs and CPUs and a PC. A block diagram of the receiver is shown in Fig.2. With the use of a YIG (Yttrium Iron Garnet) tunable filter, carrier frequency could be varied and it corresponded with various experimental conditions. Due to its high cost, the YIG tunable filter is generally used in spectrum analyzers or military applications. However, this filter was adopted in this system because it offers the advantage of variable frequency range. The prototype receiver obtains an IF output of 40 MHz corresponding to an input in the range of 2 ~ 8 GHz for every four channels. The phase adjustment of ±90° is possible for proofreading between channels and the amplitude can be adjusted within the range of 0 ~ –20 dB. The circuit is composed of a two-stage mixer and amplifiers and filters. The carrier frequency can be varied according to the input frequency of the LO and the voltage of the YIG tunable filter can be controlled. Figure 3 shows A/D and D/A converter and digital processors. The IF signal is generated from D/A converters and sampled using A/D converters. The real-time processing is possible using the FPGAs on the borads and using, and off-line processing is also possible controlling with TCP/IP using a PC. Using the off-line processing, every algorithm is examined on the system.

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3. Measurement in an Indoor Environment

4×4 MIMO transmission experiment at 5GHz is performed in an indoor environment as a system evaluation. Figure 4 shows the environment. The transmitting point and receiving point is face to face with 3 m and both of the transmitting antenna and reviving antenna is 4-element linear array antennas with half-wavelength intervals. The cannel estimation is using 50 symbol preamble symbols from each element which is the part of 9th order M-sequence and data symbol is 300 symbol random data. The symbol rate is 4MHz and one packet contains 500 symbols. Figure 5 shows the IQ constellation. (a) is the constellation of a element with no processing and (b) is the constellation of a separated sequence using Zero-forcing method. The MIMO processing performed correctly.

4. Conclusion

In this paper, the 4×4 MIMO prototype system constructed with a 4-channel transmitter and receiver, D/A and A/D converters was introduced. 4×4 MIMO transmission experiment at 5GHz was performed in an indoor environment as a system evaluation. The MIMO processing performed correctly.

References

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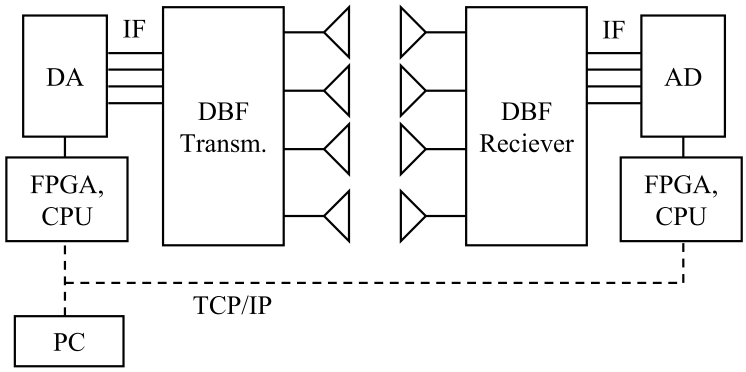
Table 1 Specification of the 4×4 MIMO Prototype System

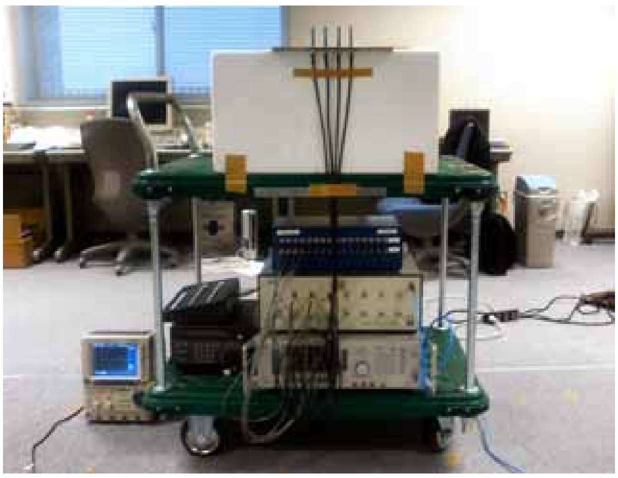
RF part	Carrier frequency	2~8 GHz (tunable)
	Number of channels	4
	IF frequency	1st: 160.7MHz, 2nd:10.7MHz (transmitter) 1st: 160MHz, 2nd: 40MHz (receiver)
	Bandwidth	5MHz
	Gain control	0 ~ –20dB
	Phase control	±90°
Digital part	D/A converter	DAC904 (Burrbrown), 100MHz 14bit (D/A)
	A/D converter	AD9245 (Analog Device), 32MHz, 14bit (A/D)
	FPGAs	ALTERA STRATIX EP1S40(1020pins, 773 I/O) 1 Mega Gates, 3,423,744 memory bits
	CPU	HITACHI SH4, 200 MHz, 360 MIPS, 1.4 GFLOPS
	SDRAM	S133-512MZ (I-O DATA), 512MB

Table 2 Measurement parameters

RF Frequency	5 GHz
Antenna	4 element linear array antennas (half-wavelength intervals)
Moduration	QPSK
Preamble	50 symbol (9thM-seq.)/ channel



(a) Construction



(b) General view

Fig.1: 4×4 MIMO Prototype system

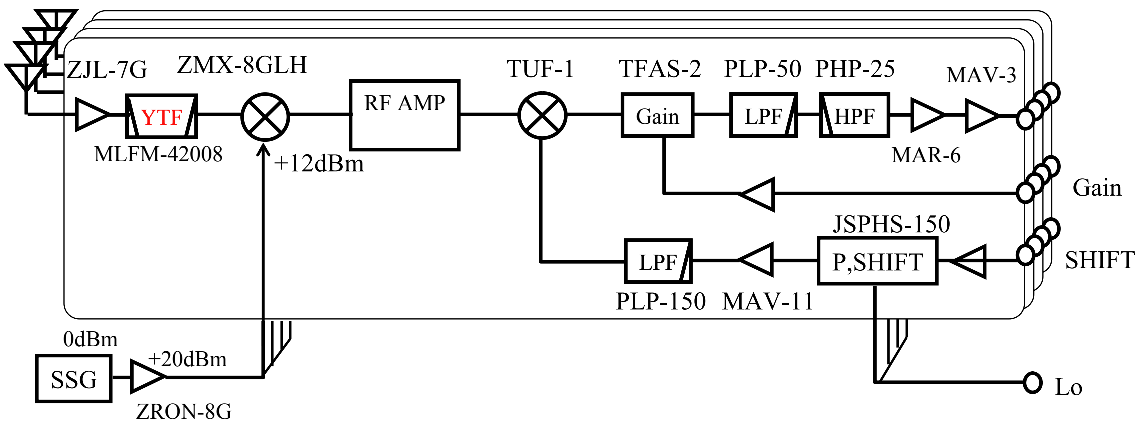


Fig. 2: Block diagram of the DBF receiver.

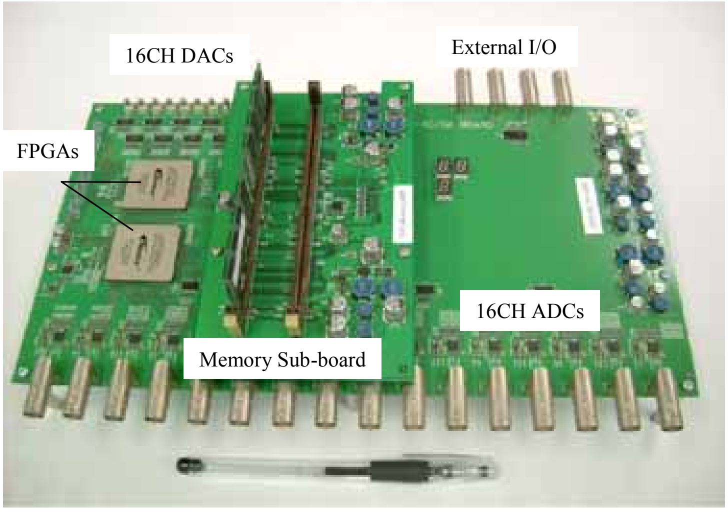


Fig. 3: A/D and D/A converter and digital processors.

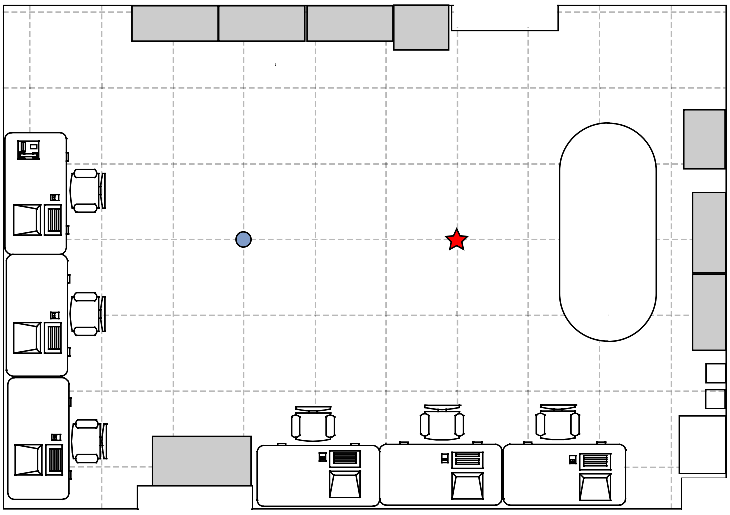
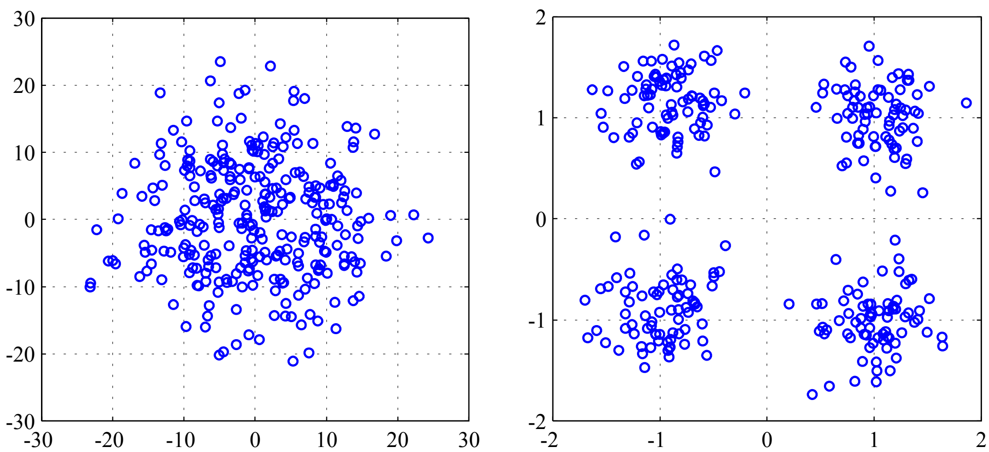


Fig.4: Measurement environment (●: receiving point, ★: transmitting point).



(a) Before processing (single element). (b)After processing (Zero-forcing).

Fig.5: IQ constellation (4×4 measurement, QPSK)