Application and Estimation of Relaxation-Based Simulation Techniques to Interconnect and Plane Networks

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Abstract— This paper describes an application of relaxation-based simulation techniques to interconnect and plane networks and its estimation. First, the characteristics of the power/ground plane networks are shown. Next, the formulation of the plane network by nodal analysis (NA) method is suggested. Furthermore, application and estimation results of the relaxation-based numerical analysis are shown. Finally, it is confirmed that the relaxation-based methods are much more efficient than the conventional methods.

1. Introduction

With the rapid progress of circuit integration technologies, high-speed and high-density electric circuits have been designed. Then, a variety of effects on the plane and the interconnects such as signal delay, reflection, crosstalk, and simultaneous switching noise (SSN) which is induced by the voltage fluctuations on the power/ground planes lead to the unexpected errors on circuits [1][2]. Therefore, it becomes important to verify the electric circuit behaviors including these effects in the early stage of circuit design flow. In order to analyze these effects in detail, the modeling and simulation methods, which can deal with 2- and 3-dimensional structures, are required for interconnects and substrates. As one of the remedies for this issue, we have also developed 3-dimensional full-wave EMI simulator BLESS which is based on the parallel and distributed 3-dimensional FDTD method, and this simulator has been quite frequently used for the practical design routinely for these several years [3][4].

In order to simulate exactly the behaviors of interconnects and planes, an enormous number of parasitic elements have to be considered. Then, if the parasitic elements are added to the net-list, SPICE simulation is a very time consuming task. Therefore, fast simulation method different from SPICE-like ones are strongly demanded.

In this paper, some simulation techniques, such as a class of relaxation methods and latency insertion method, are discussed for the efficient analyses of interconnects and planes, and they are compared with the conventional SPICE-like ones.

2. Modeling of Plane Networks

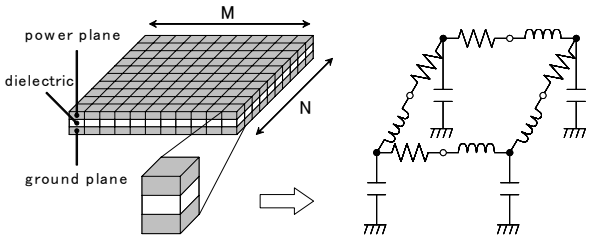


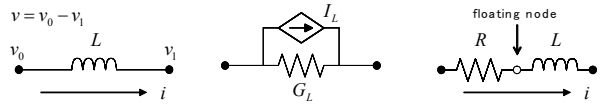
Fig. 1: (a) Discretized model of power/ground plane. (b) Equivalent circuit of a unit cell.

In general, the PCB (printed circuit board) and package have the layer structures. To deal with the high-speed interconnects, a conductor line along which the high-speed signal propagates must be placed on the opposite position of the solid ground plane. This condition should be similar to the power planes, that is to say, the power and ground plane should be face to face each other. A typical example of the power/ground plane is illustrated in Fig. 1. Fig. 1(a) shows the discretized model and this is frequently modeled by the equivalent circuit which is composed of a large number of the unit cells including passive RLC elements as shown in Fig. 1(b) [5].

As described above, the power/ground plane can be modeled by an enormous number of RLC elements. However, when the network is modeled as RLC circuit, the circuit equation based on MNA method becomes

very large-scale. This means that the simulation is also the time-consuming task. Therefore the conventional method such as SPICE-like simulation would not be practical.

3. Network Formulation by Nodal Analysis



(a) (b) (c)

Fig. 2: Equivalent circuit of inductor.

In Nodal Analysis (NA) method, all of the node voltages in the network are defined as unknown variables and then, the following equation (1) is derived by applying Kirchhoff's current law (KCL) to each node.

$$\mathbf{Gv} = \mathbf{I}, \tag{1}$$

where $\mathbf{G}$ is the conductance matrix, $\mathbf{v}$ is the unknown node voltage vector and $\mathbf{I}$ is the current source vector.

In this formulation, the stamps of an inductor and a capacitor are added to the circuit equation via the following process. For example, for an inductor shown in Fig. 2(a), applying the trapezoidal formula

$$x^{n+1} = x^n + h\left(\frac{\dot{x}^{n+1} + \dot{x}^n}{2}\right),$$

and solving for the unknown current leads to

$$i^{n+1} = G_L v^{n+1} + I_L, \tag{2}$$

where $G_L = h/2L$, $I_L = G_L v^n + i^n$ and h is a time step size. In a similar manner, a capacitor can be transformed into

$$i^{n+1} = G_C v^{n+1} + I_C, \tag{3}$$

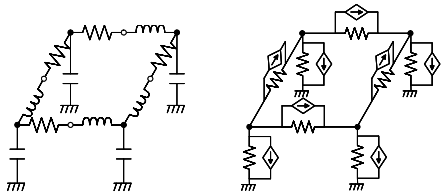
where $G_C = 2C/h$ and $I_C = -\left(G_C v^n + i^n\right)$. (2) and (3) mean that an inductor and a capacitor can be replaced with the equivalent circuit shown in Fig. 2(b). This equivalent circuit is called a companion model. Using the companion model, the circuit equation is formulated by inserting G_L and I_L corresponding to the inductor and G_C and I_C corresponding to the capacitor into the conductance matrix and the current source vector respectively.

In the case of dealing with the branch shown in Fig. 2(c), which consists of serial inductor and resistor, this should be regarded as a branch. Then, applying KVL and the trapezoidal formula to the branch and solving the equation for the unknown current leads to

$$i^{n+1} = G'_L v^{n+1} + I'_L, \tag{4}$$

where $G'_L = h/(hR + 2L)$ and $I'_L = G'_l v^n + \{(-hR + 2L)/(hR + 2L)\} i^n$. Because (4) is the same form to (2), the equivalent circuit is also same configuration to Fig. 2(b). This means that the branch shown in Fig. 2(c) can be represented by the branch in Fig. 2(b) according to NA method. By using this branch modeling and the nodal analysis method, the size of circuit equation can be reduced compared with MNA (modified nodal analysis) method. As described in 2, the power/ground network has the same branch configuration. Thus, it is expected that the NA method is very available for the simulation of power/ground networks.

In order to apply NA method to the plane network analysis, the unit cell in Fig. 3(a) is replaced by the equivalent companion model shown in Fig. 3(b). By using NA formulation with the companion models, floating nodes are removed as described above. Furthermore, note that every node in the circuit which has unknown voltage variable provides a capacitive path to the ground. Therefore, G_C corresponding to an equivalent resistor of a capacitor connected to the ground is substituted to the diagonal position of the conductance matrix $\mathbf{G}$ in (1). Because of this reason, the matrix $\mathbf{G}$ is diagonally dominant.



(a) (b)

Fig. 3: (a) Unit cell in the plane circuit. (b) Equivalent model to a unit cell.

4. Numerical Methods

4.1. Gauss-Seidel Relaxation Method

Because the high-speed interconnect and plane networks are modeled with passive RLC elements, the circuit equation becomes a linear simultaneous system of equations. Here consider to apply the relaxation-based numerical method to interconnect and plane network analysis. Furthermore, consider to solve a linear system $\mathbf{Bx}=\mathbf{r}$ for the unknown variable vector $\mathbf{x}$. In this method, an initial guess is assumed for the iteration formula and the successive approximate solutions obtained by iterative calculations converge to the true solution step by step. The (k+1)-th approximate solution by the Gauss-Seidel method, which is one of the relaxation methods, is written by

$$\mathbf{x}^{(\mathbf{k+1})}=\left(\mathbf{L}+\mathbf{D}\right)^{-1}\left(-\mathbf{U}\mathbf{x}^{(k)}+\mathbf{r}\right), \qquad (5)$$

where k is the iteration count, $\mathbf{D}$ is the diagonal part of the coefficient matrix $\mathbf{B}$, and $\mathbf{U}$ and $\mathbf{L}$ consist of upper or lower triangular elements of $\mathbf{B}$ without its diagonal elements respectively. By iterative calculations with (5), a linear simultaneous system of equations is solved.

It is well-known that the relaxation method has the serious convergence problems dependent on the characteristics of the coefficient matrix $\mathbf{B}$ [6]. One of the sufficient conditions is the diagonal dominance. For the n × n matrix $\mathbf{B}$ which consists of real number elements, if the absolute value of an arbitrary diagonal element is larger than the sum of the absolute values of off-diagonal elements in the same row or equal, $\mathbf{B}$ is diagonally dominant. In addition, especially if the absolute value of an arbitrary diagonal element is strictly bigger than the sum of the absolute values of off-diagonal elements in the same row, $\mathbf{B}$ is considered connectedly diagonally dominant. It is known that approximate solutions by iterative calculations by the Gauss-Seidel method converges to the true solution if the matrix $\mathbf{B}$ is diagonally dominant. As described above, the conductance matrix $\mathbf{G}$ of the NA formula for the plane circuit which corresponds to the coefficient matrix $\mathbf{B}$ is connectedly diagonally dominant. Therefore, it is expected that the circuit equation is solved efficiently by applying the Gauss-Seidel relaxation method.

4.2. Latency Insertion Method (LIM)

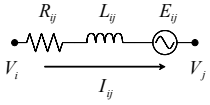


Fig. 4: Branch topology for LIM.

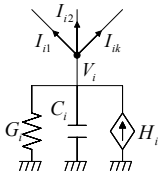


Fig. 5: Node topology for LIM.

In the standard circuit simulation algorithms, the currents and voltages are updated at the same time by calculating the circuit equation. In the LIM algorithm [7], in contrast, the current and voltage variables are collocated in half time steps and then all of the branch currents and the node voltages are calculated in turn as the time progresses. In order to generate the updating formulas for LIM, a topology of the network has to be satisfied with the requirements: Each branch in the network must contain an inductance as shown in Fig. 4 and each node in the network must provide a capacitive path to the ground as shown in Fig. 5. Otherwise, a small inductor is inserted into the branch and a small shunt capacitor is added at that node respectively [7].

By applying KVL to a branch shown in Fig. 4 and solving for the unknown current leads to

$$I_{ij}^{n+1}=I_{ij}^{n}+\frac{\Delta t}{L_{ij}}\left(V_i^{n+\frac{1}{2}}-V_j^{n+\frac{1}{2}}-R_{ij}I_{ij}^{n}+E_{ij}^{n+\frac{1}{2}}\right), \qquad (6)$$

where E is the voltage source. By applying KCL to a node shown in Fig. 5 and solving for the unknown voltage leads to

$$V_i^{n+\frac{1}{2}}=\frac{\dfrac{C_i V_i^{n-\frac{1}{2}}}{\Delta t}+H_i^{n}-\sum_{k=1}^{M_i}I_{ik}^{n}}{\dfrac{C_i}{\Delta t}+G_i}, \qquad (7)$$

where H is the current source. By this formulation, the calculation cost proportional to the number of branches and nodes. Therefore, the LIM algorithm can reduce the CPU time for the transient simulation compared to the conventional methods based on SPICE-like algorithms which require the matrix solver.

5. Numerical Results

In 5, we try to apply the relaxation method and LIM to the numerical analyses of the plane networks and estimate the accuracy and efficiency. First, in order to

verify accuracy of the relaxation-based technique, the transient responses of node voltages in the 4 × 4 plane circuit have been simulated and the obtained waveform response is illustrated in Fig. 6. In order to estimate the accuracy, the waveform result by HSPICE is also shown in Fig. 6. Both waveforms indicate good agreement. Therefore, the accuracy of the relaxation method is comfortable.

Next, comparison results of the simulation costs are shown in Table 1, and Fig. 7 shows the CPU times vs. network scale. In Table 1, "NA+GS" means the relaxation-based technique and "MNA+LU" means the conventional one based on the MNA method. By comparison between these techniques, it is confirmed that the relaxation method and LIM make the transient simulation for a large networks be faster than the conventional one. In addition, from Fig. 7, increasing rate of the simulation time for the relaxation-based methods is linear, in contrast, the conventional one is increasing according to $O\left(n^{1.5\sim 2}\right)$. Therefore, the relaxation-based methods enable to do the fast transient simulation analysis even if in the cases of the simulations of plane circuits whose sizes are very large.

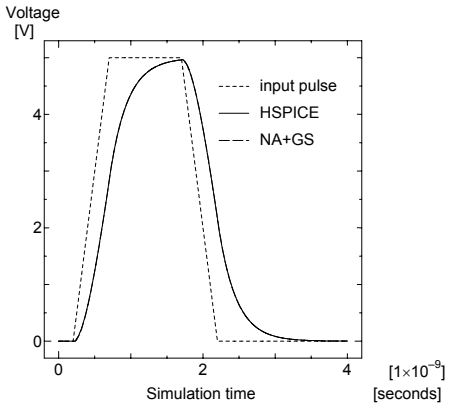


Fig. 6: Waveform results for 4 × 4 plane circuit obtained by HSPICE and the relaxation method.

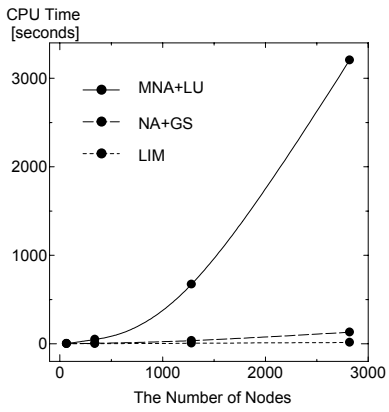


Fig. 7: CPU costs vs. network scale.

Table 1: Simulation costs of the plane circuits by three methods. (seconds)

size (cells)	nodes	NA+GS	LIM	MNA+LU
4×4	65	1.08	0.14	3.08
10×10	341	6.08	1.75	49.16
20×20	1,281	35.97	6.27	672.56
30×30	2,821	130.95	15.16	3206.56

6. Conclusions

In this paper, we described the application of relaxation-based methods, such as Gauss-Seidel method and Latency Insertion method, to the power/ground plane simulations and its estimation. In our methods, the given network is formulated by NA method with the companion models and numerically analyzed by the relaxation-based methods. By comparisons of the suggested methods with the conventional MNA-based SPICE-like ones, it has been confirmed that the relaxation-based methods enable to do the fast transient analysis of the plane circuit with good accuracy. As a result, we have confirmed that the relaxation based methods are useful for the plane circuit simulation in the time domain.

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