# Imprementation of Design Tool for Class E Switching Circiuts Using SPICE 

Hiroo Sekiya, Tooru Ezawa, and Takashi Yahagi<br>Graduate School of Advanced Integration Science, Chiba University<br>1-33, Yayoi-cho, Inage-ku, Chiba, 263-8522 JAPAN<br>Email: sekiya@faculty.chiba-u.jp


#### Abstract

This paper presents a design tool for class E switching circuits using Spice. This design tool is implemented by using the software of PSpice and OPTIMUS. Because of automatic calculations of bias points included in PSpice, two kinds of algorithm are prepared. One is a fast algorithm for the circuit design with ideal switch models, and the other is a slow algorithm with active device models. Both algorithms achieve high accurate designs for class E switching circuits. Moreover, easy operation is realized for the designers by using graphical user interface in OPTIMUS. We can show the validity of the proposed design procedure from two design examples.


## 1. Introduction

Class E switching-mode [1]-[7] have become increasingly valuable building blocks in many applications, e.g., radio transmitters and switching-mode dc power supplies. Because of class E switching, namely, both zero voltage and zero slope of voltage switching, the efficiency of energy conversion is very high at high frequencies. Class E switching has advantage for tolerance of elements because of zero slope of voltage switching, namely, high power conversion efficiency can be kept even if there are tolerances on each element.

Since the introduction of the class E amplifier that is one of typical class E switching circuits, many design procedure of this circuit have appeared [1]-[7]. The design procedures in [4] and [5] are very simple and easy design procedure compared with above schemes. These schemes require only circuit equations and the other processes of the design is carried out with aid of computer. The design scheme in [4], however, requires that circuit equations have to be piecewise linear expressions since linear differential equations are solved numerically using eigenvalues of matrix from circuit equations. On the other hand, the scheme in [5] and [6] allows any expressions of circuit equations.

By the way, many designers would like to use circuit simulators, e.g., Spice to design the class E circuits since it is spiny to formulate circuit equations, especially, for high dimensional circuits. Moreover it is also a reason that circuit simulators have rich element models, namely, MOSFETs, diodes, and so on. It is common knowledge for the designers that the effects of parasitic resistance, parasitic capacitance and its nonlinearities and drain current fall time are quite important and should be taken into account for
the design of class E switching circuits. The first barrier to solve this problem is how to make a model of active devices since accuracy of the design values depends on that of the element models. From this point of view, it is recognized that the device models in circuits simulator is powerful and helpful tools. Any design procedure presented until now, however, never allows to use a circuit simulator for the design of class E switching circuits. That is because all design procedures require explicit circuit equations. If a design procedure allows implicit circuit equations, the designers can use circuit simulator for the design of class E switching circuits. This may provides simpler and easier design and class E switching technique is more familiar for us.

This paper presents a novel design procedure for class E circuits for using Spice. Because of automatic calculations of bias points included in PSpice, long transient simulation is applied. The proposed design algorithms are implemented by using the software of PSpice ${ }^{1}$ and OPTIMUS ${ }^{2}$ The implemented design tool achieves high accurate designs for class E switching circuits. Moreover, easy operation is realized for the designers by using graphical user interface in OPTIMUS. We can show the validity of the proposed design procedure from two design examples.

## 2. Formulation of the Problem

In this section, the problem to derive the design values of class E switching circuits are formulated. The design problem is boils down to solve the algebraic equations.

### 2.1. Circuit Description

Let us consider a dynamic circuit described by a differential equations:

$$
\begin{equation*}
\frac{d x}{d t}=f(t, x, \lambda) \tag{1}
\end{equation*}
$$

where $t \in \boldsymbol{R}, \boldsymbol{x} \in \boldsymbol{R}^{n}$, and $\lambda \in \boldsymbol{R}^{m}$ denote the time, an $n$ dimensional state and an $m$-dimensional system parameter, respectively. In this paper, For simplicity,

$$
\begin{align*}
f: \boldsymbol{R} \times \boldsymbol{R}^{n} \times \boldsymbol{R}^{m} & \rightarrow \boldsymbol{R}^{n}  \tag{2}\\
(t, \boldsymbol{x}, \boldsymbol{\lambda}) & \mapsto f(t, \boldsymbol{x}, \boldsymbol{\lambda})
\end{align*}
$$

[^0]is assumed as $C^{\infty}$ mapping and is periodic in $t$ with period $t_{T}:$
\[

$$
\begin{equation*}
f\left(t+t_{T}, \boldsymbol{x}, \boldsymbol{\lambda}\right)=f(t, \boldsymbol{x}, \boldsymbol{\lambda}) \tag{3}
\end{equation*}
$$

\]

We also assume that (1) has a solution $\boldsymbol{x}(t)=\boldsymbol{\varphi}\left(t, \boldsymbol{x}_{\mathbf{0}}, \lambda\right)$ defined on $-\infty<t<\infty$ with every initial condition $x_{0} \in$ $\boldsymbol{R}^{n}$ and every $\boldsymbol{\lambda} \in \boldsymbol{R}^{m}: \boldsymbol{x}(0)=\varphi\left(0, x_{\mathbf{0}}, \lambda\right)=\boldsymbol{x}_{\mathbf{0}}$.

### 2.2. Steady-state Conditions

By the periodic hypothesis (3), we can naturally define a $C^{\infty}$ diffeomorphism $T$ from state space $\boldsymbol{R}^{n}$ into itself :

$$
\begin{align*}
T: \boldsymbol{R}^{n} & \rightarrow \boldsymbol{R}^{n} \\
x_{0} & \mapsto T\left(x_{0}, \lambda\right)=\varphi\left(t_{T}, x_{0}, \lambda\right) . \tag{4}
\end{align*}
$$

The mapping $T$ is often called the Poincaré mapping.
If a solution $\boldsymbol{x}(t)=\boldsymbol{\varphi}\left(t, \boldsymbol{p}_{\mathbf{0}}, \lambda\right)$ is periodic with period $t_{T}$, the point $\boldsymbol{p}_{\mathbf{0}} \in \boldsymbol{R}^{n}$ is a fixed point of $T$ :

$$
\begin{equation*}
T\left(p_{0}, \lambda\right)=p_{0} . \tag{5}
\end{equation*}
$$

If $\boldsymbol{p}_{\mathbf{0}}=\boldsymbol{x}_{\mathbf{0}}$, (5) corresponds to the boundary conditions for a steady state. The numerical derivation of boundary conditions from (5) is called as shooting method, which is generally the application of Newton's method to (5).

### 2.3. Other Conditions

For the designs of class E switching circuits, we should consider class E switching conditions, a specified output power, maximum voltage, and so on. If the number of conditions is $N(\leq m)$, the conditions that consist of each condition $g_{k}$ are expressed as

$$
G\left(\boldsymbol{x}_{\mathbf{0}}, \lambda\right)=\left[\begin{array}{c}
g_{1}\left(\boldsymbol{x}_{\mathbf{0}}, \boldsymbol{\lambda}\right)  \tag{6}\\
g_{2}\left(\boldsymbol{x}_{\mathbf{0}}, \lambda\right) \\
\vdots \\
g_{N}\left(\boldsymbol{x}_{\mathbf{0}}, \lambda\right)
\end{array}\right]=\mathbf{0}, \quad \in \boldsymbol{R}^{N} .
$$

In this case, we can find $N$ design parameters. Therefore, the other $(m-N)$ parameters must be given as the design specifications. We recognize that the design of the amplifier boils down to the derivation of the solutions of the algebraic equations (5) and (6).

## 3. Proposed Design Procedure

In this section, the design procedure with implicit circuit equations is proposed. We apply numerical approximations of partial differential to Jacobian matrix whose derivations require no explicit circuit equations.

We consider two cases in order to derive the solutions of (5) and (6). They are classified whether initial condition $\boldsymbol{x}_{\boldsymbol{0}}$ can be given arbitrarily or not. Generally, Spice does not allow users to give the rigorous initial conditions when active devices are included in the circuit configurations. This means that Spice have a automatic function of "Searching


Figure 1: Flowchart of the proposed algorithm.
bias point". In this paper, the case the initial condition $\boldsymbol{x}_{\mathbf{0}}$ cannot be given is considered. If ideal switching models is used instead of active device models, the design procedures [6] can be applied since the Spice skips the function of "Searching bias point".

The flowchart of the proposed algorithm is shown in Fig. 1. Compared with the algorithm in [6], a long transient simulation is applied to (1) in order to derive the waveforms in the steady state in stead of shooting method. Now, the transient simulation is carried out for $0 \leq t \leq M t_{T}$, where $M$ is a natural number that is enough large to achieve $\varphi\left(M t_{T}\right)-\varphi\left((M-1) t_{T}\right) \ll 1$. Moreover, it is assumed that the all conditions in (6) are acquired from the steady state waveforms, namely, from the waveforms for $(M-1) t_{T} \leq$ $t \leq M t_{T}$. Then, the design values can be derived by solving only (6) that is rewritten as the following equation,

$$
F_{1}(\lambda)=G(\lambda)=\left[\begin{array}{c}
g_{1}(\lambda)  \tag{7}\\
g_{2}(\lambda) \\
\vdots \\
g_{N}(\lambda)
\end{array}\right]=\mathbf{0}, \quad \in \boldsymbol{R}^{N}
$$

Note that $g_{k}$ is function of only $\lambda$. The flowchart of the proposed design prprocedure is almost similar to that in [6]. We define $\lambda_{u} \in \boldsymbol{R}^{\boldsymbol{N}}$ as

$$
\begin{align*}
\lambda_{u}= & \left\{\lambda_{u 1}, \lambda_{u 2}, \cdots, \lambda_{u N} \mid \lambda_{u k}(k=1,2, \cdots, N)\right. \\
& \text { are unknown design parameters in } \lambda .\} \tag{8}
\end{align*}
$$

The equations (7) are solved by using Newton's method with the iterative computations

$$
\begin{equation*}
\lambda_{u}{ }^{k+1}=\lambda_{u}{ }^{k}-\frac{F_{1}\left(\lambda_{u}{ }^{k}\right)}{F_{1}^{\prime}\left(\lambda_{u}{ }^{k}\right)} \tag{9}
\end{equation*}
$$

for $\left\|\boldsymbol{u}^{k+1}-\boldsymbol{u}^{k}\right\|<\delta$. The Jacobian matrix $F_{1}^{\prime}$ is given as follows [6].

When a new vector $\boldsymbol{u}_{\varepsilon i}$ is defined as

$$
\begin{equation*}
\boldsymbol{u}_{\boldsymbol{\varepsilon i}}=\left[u_{1}, u_{2}, \cdots, u_{i}+\varepsilon, \cdots, u_{n+N}\right], \tag{10}
\end{equation*}
$$

the approximate values of partial differentials in $F_{1}^{\prime}\left(\boldsymbol{u}^{k}\right)$ are calculated by using the following approximation;

$$
\begin{align*}
\frac{\partial T_{j}\left(\boldsymbol{u}^{k}\right)}{\partial u_{i}} & =\frac{T_{j}\left(\boldsymbol{u}_{\boldsymbol{\varepsilon i}}^{k}\right)-T_{j}\left(\boldsymbol{u}^{k}\right)}{\varepsilon} \\
\frac{\partial g_{l}\left(\boldsymbol{u}^{k}\right)}{\partial u_{i}} & =\frac{g_{l}\left(\boldsymbol{u}_{\boldsymbol{\varepsilon i}}^{k}\right)-g_{l}\left(\boldsymbol{u}^{k}\right)}{\varepsilon} \tag{11}
\end{align*}
$$

In (11), $i=1,2, \cdots, n+N, j=1,2, \cdots, n, l=1,2, \cdots, N$, and $\varepsilon \ll 1$ means a minute variation. By calculating this approximation, $T_{j}\left(\boldsymbol{u}_{\boldsymbol{\varepsilon}}{ }^{k}\right)$ and $g_{j}\left(\boldsymbol{u}^{k}\right)$ can be derived from the responses $\varphi\left(t, \boldsymbol{u}_{\varepsilon i}{ }^{k}\right)$ that is same as one for derivations of $F_{1}(\boldsymbol{u})$ by substituting $\boldsymbol{u}_{\boldsymbol{\varepsilon} i}$ for $\boldsymbol{u}$. The circuit response $\varphi$ can be given from circuit simulator.

In Fig.1, the vector $\lambda_{u s i}$ is defined as

$$
\begin{equation*}
\lambda_{u s i}=\left[\lambda_{u 1}, \lambda_{u 2}, \cdots, \lambda_{u i}+\varepsilon, \cdots, \lambda_{n+N}\right], \tag{12}
\end{equation*}
$$

where $\varepsilon \ll 1$ means a minute variation. The disadvantage of this procedure to calculation cost is higher than the algorithm in [5] and [6] because of long transient simulations. On the other hand, the benefits of the proposed design procedure are;

1. It is unnecessary to derive the variational equations in the design procedure. If the circuit equations are implicitly formulated by using circuit simulator, all steps of the design are carried out with aid of computer. Hence, the proposed design procedure allows less effort for the designs compared with the method in [5]. This design procedure can be applied to the design with explicit circuit equations.
2. Since it is unnecessary to derive the variational equations, many kinds of conditions in (6) are specified. If the conditions are observed from the responses of the circuit, that is $\varphi$, any equations of conditions can be given. Therefore, the proposed procedure allows the statistic conditions, e.g., average output voltage, maximum drain voltage, and so on.
3. If circuit equations are identical, the accuracy of the design values are determined by $\delta$ that is a stop condition of the Newton's method. Therefore the derived design parameters are complete same as that from the procedure in [5] and [6] with same circuit equations and $\delta$. As a result, the sufficient accuracy is achieved since [5] shows that the high accurate design is achieved compared with other methods.


Figure 2: Circuit topology of class E amplifier.
4. The accuracy of circuit equations is improved in case of using circuit simulator since it provides high accurate device models. Therefore, the accuracy of design values from the proposed design procedure is also improved compared with [5] and [6] by using accurate device models.

## 4. Design Examples using PSpice

The proposed algorithm is implemented as design tool by using software "PSpice" and "OPTIMUS". PSpice is well known as one of the most popular circuit simulators and provides the numerical data of waveforms. By using the software "Orcad Capture", the circuit configuration is given to a computer graphically. OPTIMUS uses as a interface between the PSpice and the proposed algorithm. This means that the unknown parameters $\boldsymbol{u}$ or $\boldsymbol{\lambda}_{\boldsymbol{u}}$ are given from our algorithm to PSpice via OPTIMUS. The numerical data of the waveforms $\varphi$ are also given from PSpice to our algorithm via OPTIMUS. Since OPTIMUS have a function of Graphic User Interface (GUI), the specified conditions can be also given to a computer graphically. As a result, all steps of design procedure are carried out with aid of computer dialogically and simple and easy design tool can be realized.

The design example of class E amplifier is shown in this paper. Figure 2 depicts the circuit topology of class E amplifier. It consists of a dc supply voltage $V_{D}$, a dc-feed inductor $L_{c}$, a switch $S$ and a capacitor $C_{S}$ shunting the switch, a series resonant circuit $L_{0}-C_{0}$, and an output resistor $R$. An example of the waveforms of class E amplifier is shown in Fig. 3, when switch on duty ratio is $50 \%$. The switch is driven by a driving pattern of $D_{r}$ in Fig. 3. If the dc-feed inductance $L_{c}$ is large, the input current $i_{c}$ of the amplifier is approximately constant, which is equal to its dc component. If the loaded quality factor $Q$ is high ( $Q \geq 5$ ), the current $i_{o}$ through the $L C$ resonant circuit is approximately a sine wave. As shown in Fig. 3, while the switch is off, the current through the shunt capacitor produces the voltage $v_{s}$ across the switch. While the switch is on, it is flowing through the switch as $i_{S}$. Since the switching loss


Figure 3: Nominal waveform of class E amplifier with a MOSFET model from PSpice simulation. The design parameters are given by the proposed design procedure in Sec. 4.2.
is reduced to zero by the operating requirements of zero and zero slope of switch voltage ( $v_{s}=0$ and $d v_{s} / d t=0$ ) at the turn on transition, called class E switching conditions, the theoretical efficiency of class E amplifier is $100 \%$.

The design of class E amplifier modeled in Fig. 2 is carried out. This model includes an active device, namely MOSFET. Therefore, the exact initial conditions $\boldsymbol{x}_{\boldsymbol{0}}$ cannot be given for PSpice because of calculations of bias point. Therefore, the proposed design algorithm should be applied to this design. The design specifications are as follows; the operating frequency $f=1.0 \mathrm{MHz}$, the dc supply voltage $V_{D}=5.0 \mathrm{~V}$, output resistor $R=5.0 \Omega$, the dc-feed inductance $L_{c}=0.8 \mathrm{mH}$, the resonant capacitance $C_{0}=3.5 \mathrm{nF}$. Moreover, IRF530 MOSFET model is used for the actice device, which includes on resistance, drainsource parasitic capacitance with its nonlinearity, drain current fall time and so on. It is unnecessary for the designer to make a model of these characteristics since the proposed design procedure uses the MOSFET model from PSpice library. The results of the design values are $L_{0}=8.19 \mathrm{nH}$ and $C_{S}=5.49 \mathrm{nF}$. The waveforms by PSpice are given in Fig. 3 . From the waveform of $v_{S}$ in this figure, it is also confirmed that class E switching conditions are satisfy and the validity of the proposed design procedure can be shown. The calculations times are three times as long as that in [6] because of the long transient simulation.

## 5. Conclusion

This paper has presented a novel design procedure for class E circuits for using Spice. Because of automatic calculations of bias points included in PSpice, long transient simulation is applied. The proposed design algorithms are implemented by using the software of PSpice and OPTIMUS. The implemented design tool achieves high accurate designs for class E switching circuits. Moreover, easy operation is realized for the designers by using graphical user interface in OPTIMUS. We can show the validity of the proposed design procedure from two design examples.

## Acknowledgments

This research was partially supported by Saneyoshi Scholarship Foundation and Grant-in-Aid for scientific research (No. 17760296 and 18560269) of JSPS. The authors special thanks to Cybernet Inc., Japan for his kind help about this research.

## References

[1] N. O. Sokal and A. D. Sokal, "Class E - A new class of high-efficiency tuned single-ended switching power amplifiers, " IEEE J. of solid-state circuits, vol. SC-10, no. 3 pp. 168-176, June 1975.
[2] C. P. Avratoglou, N. C. Voulgaris, F. I. Ioannidou, "Analysis and design of a generalized class E tuned power amplifier," IEEE Trans. Circuits syst., vol. CAS36, no. 8, pp. 1068-1079, Aug. 1989.
[3] N. O. Sokal, "Class-E RF power amplifiers", $Q E X$, no. 204, pp. 9-20, Jan./Feb. 2001.
[4] P. Reynaert, K. L. R.Mertens, M. S. J. Steyaert, "A state-space behavioral model for CMOS class E power amplifiers," IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 22, no. 2, pp. 132 - 138, Feb. 2003.
[5] H. Sekiya, I. Sasase and S. Mori, "Computation of design values for class E amplifiers without using waveform equations, " IEEE Trans. Circuits and Systems, vol. 49, no. 7, pp. 966-978, July 2002.
[6] H. Sekiya and Y. Tanji, J. Lu, and T. Yahagi, "Design procedure for generalized class E amplifiers with implicit circuit equations," Proceedings of The 2004 International Symposium on Nonlinear Theory and Its Applications(NOLTA 2004) , pp. 303-306, Dec. 2004.
[7] T. Kawano and Y. Tanji, "Optimization of the class E amplifier using multi-level Newton method," Technical Report of IEICE, vol. 106, no. 345, NLP2006-81, pp. 23-26, Nov. 2006. (in Japanese)


[^0]:    ${ }^{1}$ Cadence Design Systems Inc.
    ${ }^{2}$ Noesis Solutions NV.

