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Noise-Induced Synchronization among Sub-RF CMOS Neural Oscillators for Skew-Free Clock Distribution

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Abstract—A possible idea is presented here for dealing with clock skew problems on synchronous digital systems. Nakao *et al.* recently reported that independent neural oscillators can be synchronized by applying temporal random impulses to the oscillators [1]. We regard neural oscillators as independent clock sources on LSIs; i.e., clock sources are distributed on LSIs, and they are forced to synchronize through the use of random noises. We designed neuron-based clock generators operating at sub-RF region (< 1 GHz) by modifying the original neuron model to a new model that is suitable for CMOS implementation with 0.25-μm CMOS parameters. Through circuit simulations, we demonstrate that the clock generators are certainly synchronized by pseudo-random noises.

1. Introduction

Synchronous sequential circuits with global clock-distribution systems are the mainstream of implementation in present digital VLSI systems where the clock distribution is the core of synchronous digital operations. Practical clocks given through external pads are distributed to sequential circuits being synchronous to the same clocks via distributed clock networks. System clocks for synchronous digital circuits must arrive at all the registers simultaneously. In practice, time mismatches of clock arrival which are called 'clock skew' occur in LSIs [2]. The major reasons for these mismatches derive from the system clock distribution (wiring defects or asymmetric clock paths), the propagation delay of the clock chip, and the clock traces on the board. The propagation delay is dependent on the fabrication process, voltage, temperature, and loading, which makes the clock skew even more complicated. Small clock skews prevent us from increasing the clock frequency, and large skews may result in severe malfunctions. Indeed clock-skew effects on the circuit performance rise as the integration density (~miniaturization) or the clock frequency increases.

To resolve these clock-skew issues, various technologies on clock distribution are widely used in present digital systems such as zero-skew clock distribution [3], inserting buffers for skew compensation [4] and controlling the clock-wire length [5]. In regular circuit structures, clock skews are effectively reduced by designing clock paths based on H trees (see [6] for details including statistical analysis). For large-scale complex clock networks, optimizing buffers in the clock distribution tree usually reduces clock skew. One possible way to cancel clock skew is to use asynchronous digital circuits where only local clocks are used instead of global system clocks [7]. However, the functions of these circuits currently cannot satisfy various sophisticated demands. Moreover, major LSI designers have recently started using advanced genetic algorithms in their post-manufacturing processes to calculate the required margin [8].

The present solutions for the skew problems may increase both the total length of clock distribution wires and the power consumption, as well as optimization and post-processing costs. In this paper, we propose another solution for the skew problems. Nakao *et al.* recently reported that independent neural oscillators can be synchronized by applying appropriate noises to the oscillators [1]. We here regard neural oscillators as independent clock sources on LSIs; i.e., clock sources are distributed on LSIs, and they are forced to synchronize with the addition of artificial (or natural if possible) noises. In the following sections, we show a modified neuron-based model that are suitable for hardware implementation, neuron-based clock generator for sub-RF operations (< 1 GHz), and circuit simulation results representing synchronous (or asynchronous) oscillations with (or without) external noises.

2. The Model

In the original model [1], FitzHugh-Nagumo neuron was used to demonstrate the noise-induced synchronization between the time courses of N trials under different initial conditions. Instead we use N Wilson-Cowan oscillators in our model that are suitable for analog CMOS implementation. The dynamics are given by

$$\frac{du_i}{dt} = -u_i + f_\beta(u_i - v_i), \tag{1}$$

$$\frac{dv_i}{dt} = -v_i + f_\beta(u_i - \theta) + I(t), \tag{2}$$

where u_i and v_i represent the system variables of the i-th oscillator, θ the threshold, $I(t)$ the common temporal random impulse and $f_\beta(\cdot)$ the sigmoid function with slope β.

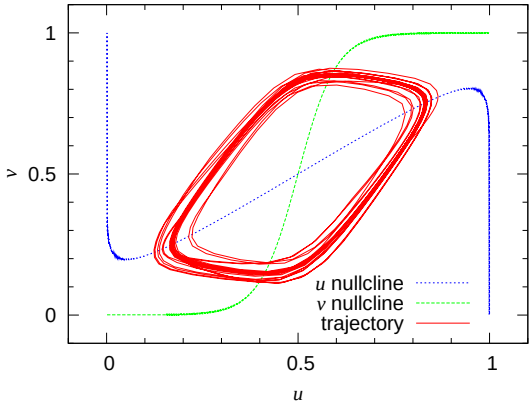

Figure 1: Nullclines and trajectories of single Wilson-Cowan type oscillator receiving random impulses.

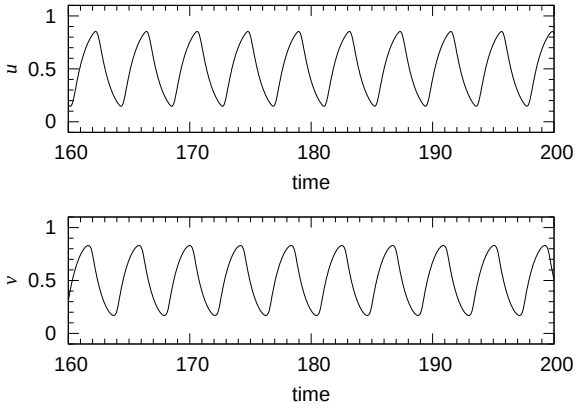

Figure 2: Time courses of system variables of single Wilson-Cowan type oscillator receiving random impulses.

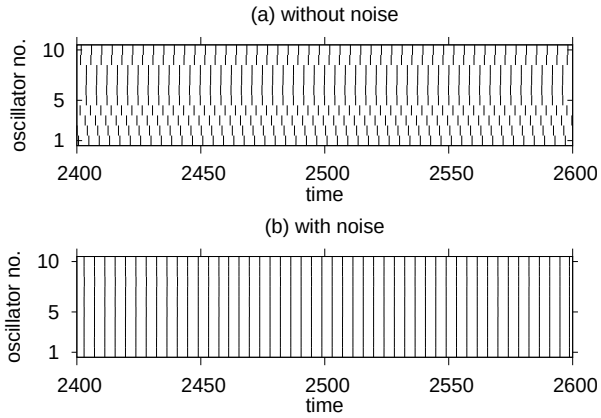

Figure 3: Raster plots of 10 oscillators. (a) independent oscillations without random impulses, (b) synchronous oscillations with random impulses.

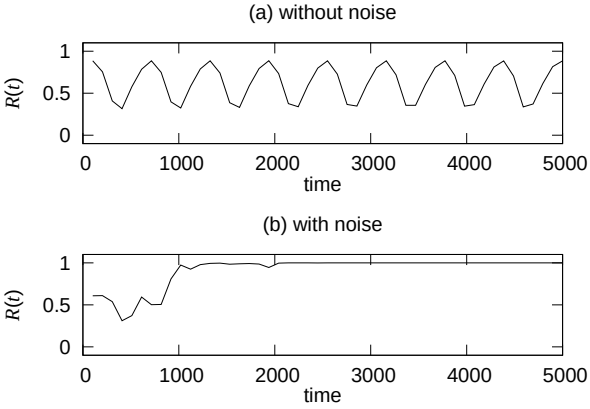

Figure 4: Time courses of order parameter values (a) without random impulses and (b) with random impulses.

Figure 1 shows numerical simulation results of a single Wilson-Cowan oscillator receiving temporal random impulses given by $I(t) = \alpha \sum_j \delta(t - t_j^{(1)}) - \delta(t - t_j^{(2)})$ where $\delta(t) = \Theta(t) - \Theta(t - w)$ (Θ, w and t_j represent the step function, the pulse width and the positive random number with $t_j^{(1)} \neq t_j^{(2)}$ for all js, respectively). The system parameters were $\theta = 0.5$, $\beta = 10$, $\alpha = 0.1$, $w = 1$, and the averaged inter-spike interval of $|I(t)|$ was set at 100. We observed the limit-cycle oscillations, and confirmed that the trajectory was certainly fluctuated by $I(t)$. The time courses of u and v are shown in Fig. 2.

We conducted numerical simulations using 10 oscillators ($N = 10$). All the oscillators have the same parameters, and accept (or do not accept) the common random impulse $I(t)$. The initial condition of each oscillator was randomly chosen. Figure 3 shows the raster plots of 10 oscillators (vertical bars were plotted at which $u_i > 0.5$ and $du_i/dt > 0$). When the oscillators did not accept $I(t)$ ($\alpha = 0$), they exhibited independent oscillations as shown in Fig. 3(a); however, all the oscillators were synchronized when $\alpha = 0.1$ as shown in Fig. 3(b). To evaluate the degree of the synchronization, we use the following order parameter:

$$R(t) = \frac{1}{N}\left|\sum_j \exp(i\theta_j)\right|,$$

where N represents the number of oscillators, i the imaginary unit and $\theta_j = \tan^{-1}[(v_j - v^*)/(u_j - u^*)]$ ((u^*, v^*) represents the fixed point of the oscillator). When all the oscillator are synchronized, $R(t)$ equals 1 because of the uniform θ_js, while $R(t)$ is less than 1 if the oscillators are not synchronized. Figure 4 shows the time courses of the order parameter values. When $\alpha = 0$, $R(t)$ was unstable and was always less than 1 [Fig. 4(a)], whereas $R(t)$ remained at 1 after it became stable at $t \approx 2000$ when $\alpha = 0.1$ [Fig. 4(b)]. These results indicate that if we implemented these oscillators as clock generators on CMOS LSIs, applying common random pulses to the oscillators could synchronize them.

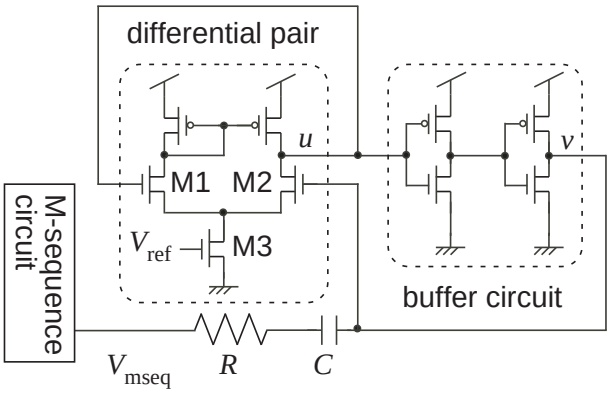

Figure 5: Wilson-Cowan circuit for sub-RF operations.

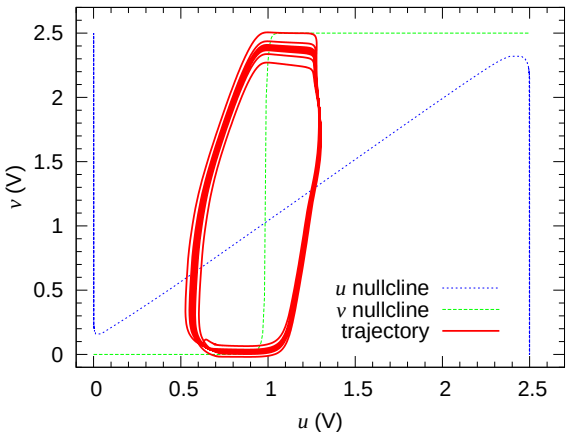

Figure 6: Nullclines and trajectories of oscillator circuit receiving pseudo-random impulse.

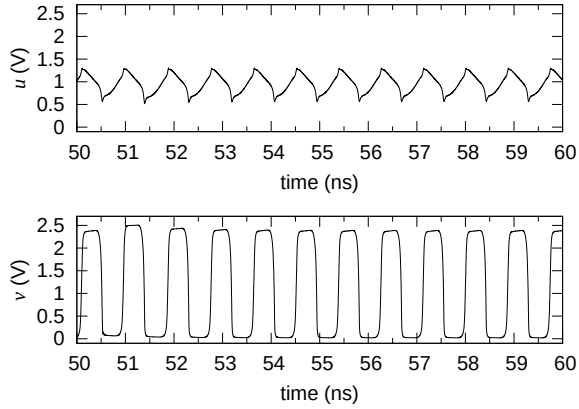

Figure 7: Time courses of system variables of oscillator circuit receiving pseudo-random impulses.

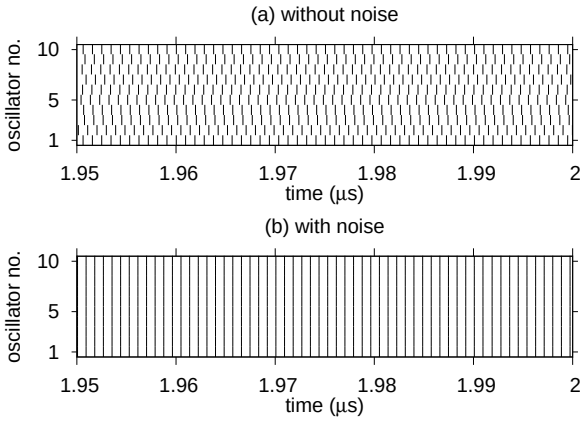

Figure 8: Raster plots of 10 oscillator circuits. (a) independent oscillations without random impulses, (b) synchronous oscillations with random impulses.

3. The circuit and simulation results

We designed a Wilson-Cowan oscillator circuit for sub-RF operations (Fig. 5). The circuit consists of a differential pair (M1 to M3) and a buffer circuit composed of two standard inverters. In the following simulations, we used TSMC's 0.25-μm CMOS parameters with $W/L = 0.36$ μm / 0.24 μm except for M3's channel length ($L = 2.4$ μm). Pseudo-random sequences (V_{mseq}) were generated using a 4-bit M-sequence circuit, and were distributed to the circuit through a RC filter. The supply voltage was fixed at 2.5 V.

Figure 6 shows SPICE results of the nullclines and trajectories receiving random impulses ($C = 10$ fF, $R = 100$ kΩ, the clock frequency of the M-sequence circuit was 50 MHz, which resulted in a 300-ns pseudo-random sequence). Time courses of u and v are shown in Fig. 7. We observed qualitatively-equivalent nullclines and trajectories to those of the Wilcon-Cowan oscillators. We confirmed the limit-cycle oscillations where the trajectory was effectively fluctuated by the M-sequence circuit with the RC filter. The oscillation frequency was about 1 GHz when the reference voltage V_{ref} was set at 1 V. Figure 8 shows the raster plots of 10 oscillator circuits (vertical bars were plotted at which $v_i > 1.25$ V and $dv_i/dt > 0$). All the circuits exhibited independent oscillations when random sequence V_{mseq} was not given to them [Fig. 8(a)], whereas they exhibited complete synchronization when V_{mseq} was given [Fig. 8(b)]. Time courses of the order parameter values were shown in Fig. 9. When random impulse was not given to the circuit, $R(t)$ was not stable and was always less than 1 [Fig. 9(a)], while $R(t)$ remained at 1 after it became stable at $t \approx 700$ μs when random impulse was given [Fig. 9(b)].

Our results indicate that if we distributed these circuits as ubiquitous clock sources on CMOS LSIs, they could be synchronized when common random impulses were given to the circuits. Although this may cancel out the present clock skew problems, device mismatches between

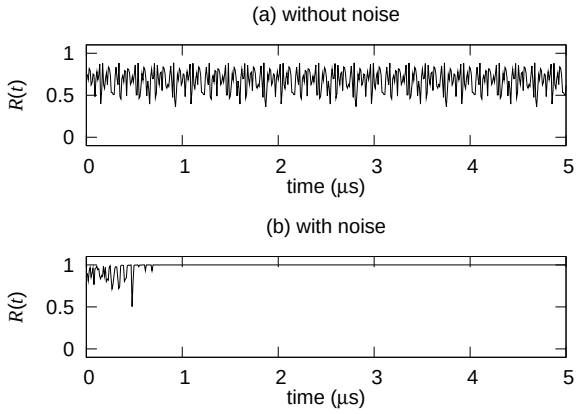

Figure 9: Time courses of order parameter values (a) without random impulses and (b) with random impulses.

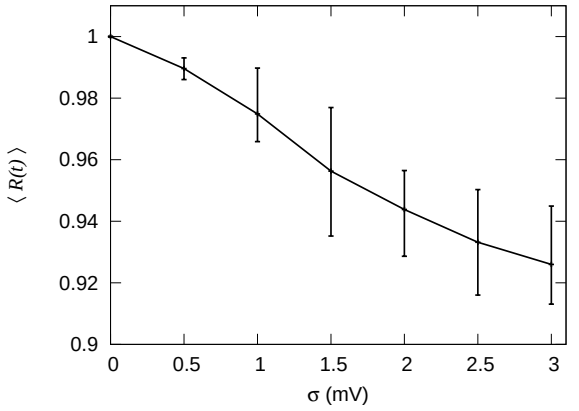

Figure 10: Synchrony dependence on parameter mismatch.

the clock sources may prevent the sources from complete synchronization. Therefore, we investigated the device-mismatch dependence of the proposed circuits. For our distributing purposes, local mismatches in a single oscillator circuit would be negligible; i.e., mismatches in a differential pair (M1 and M2) and a current mirror. Mismatches in inverters corresponding to threshold θ in Wilson-Cowan model would also be negligible because they only shift the fixed point, and do not vastly change the oscillation frequency. However, mismatches of M3 between the oscillators may drastically change each oscillator's intrinsic frequency. Therefore, we distributed threshold voltages of M3s of all the oscillators. Zero-bias threshold voltages (VTO) of M3s were randomly chosen from the Gaussian distribution (mean: 0.37 V and standard deviation: σ). Figure 10 shows the dependence of averaged order-parameter values $\langle R(t) \rangle$ (from 0 to 1 μs) on σ. We generated 10 random VTO sets for each σ, and plotted the error bars and the mean values in the figure. We confirmed that $\langle R(t) \rangle$ was gradually decreased when σ was increased.

4. Conclusion

We designed CMOS sub-RF oscillators that could be synchronized using common random impulses, based on a theory in [1]. We proposed a modified Wilson-Cowan model for implementing FitzHugh-Nagmo oscillators. We confirmed that the synchronization properties of the modified model were qualitatively equivalent to those of the original model. We then designed sub-RF oscillator circuits based on the modified model. Through circuit simulations, we demonstrated that the circuits exhibited the same synchronization properties as in the original and modified models. For our clock-distributing purposes, we investigated the synchrony dependence on device mismatches between the distributed oscillator circuits. The result showed that the synchrony was gradually decreased when variance of the mismatch was linearly increased, which indicated that our 'ubiquitous' clock sources with small device mismatches would be synchronized by optimizing our parameter sets.

References

[1] H. Nakao, K. Arai, and K. Nagai, "Synchrony of limit-cycle oscillators induced by random external impulses," *Phys. Rev. E* vol. 72, 026220, 2005.

[2] D. E. Brueske and S. H. K. Embabi, "A dynamic clock synchronization technique for large systems," *IEEE Trans. Comp., Packag., Manufact. Technol. B*, vol. 17, pp. 350-361, 1994.

[3] R. S. Tsay, "An exact zero-skew clock routing algorithm," *IEEE Trans. on Comp.-Aided Design of Integrated Cir. Syst.*, vol. 12, no. 2, pp. 242-249, 1993.

[4] R. B. Watson, Jr., and R. B. Iknaian, "Clock buffer chip with multiple target automatic skew compensation," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1267-1276, 1995.

[5] T. -H. Chao, Y. -C. Hsu, J. -M. Ho, and A. B. Kahng, "Zero skew clock routing with minimum wirelength," *IEEE Trans. Circuits and Systems II*, vol. 39, no. 11, pp. 799-814, 1992.

[6] M. Hashimoto, T. Yamamoto, and H. Onodera, "Statistical analysis of clock skew variation in H-tree structure," *IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences*, vol. E88-A, no. 12, pp. 3375-3381, 2005.

[7] C. J. Myers, *Asynchronous Circuit Design*, Wiley-Interscience, 2001.

[8] E. Takahashi, Y. Kasai, M. Murakawa and T. Higuchi, "Post-fabrication clock-timing adjustment using genetic algorithms," *IEEE J. Solid-State Circuits*, vol. 39, no. 4, pp. 643-649, 2004.