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WTA-based Switching Strategy for Paralleled DC-DC Converters

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Abstract—This paper studies switching rules of paralleled dc-dc converters. The switching rules are based on the winner-take-all function and can realize multi-phase synchronization automatically. It is suitable for efficient current sharing with lower ripple. Using simple piecewise constant model, we can analyze existence and stability of desired operation. Presenting a simple test circuit, typical dynamics can be confirmed experimentally.

1. Introduction

Paralleled dc-dc converters (PDC) have been studied from both practical and fundamental viewpoints. The PDC have common advantages of parallel systems such as improvement of reliability and fault tolerance. One important ability of the PDC is lower voltages with higher current capabilities in the next generation micro-processors [1] [2]. In order to reduce size and losses of the filtering stages, sharing output current with the lower ripple is required. In PDC, several switching control techniques have been considered for efficient power supplies: digital logical control [1], sliding surface control [3] wireless PWM control [4] and so on. On the other hand the PDC are nonlinear dynamical system having rich phenomena [8]. For example, PDC exhibits multi-phase synchronization that can be changed into a variety of periodic/chaotic phenomena. However, analysis of such dynamics is not sufficient as compared with single dc-dc converters [7].

This paper studies switching strategy for current-mode control of PDC. In the PDC, one dc source is applied to one load via N buck converters. We present two kinds of switching strategy based on dynamic winner-take-all (WTA) function. As parameters are selected suitably, the WTA-based switching can achieve N-phase synchronization (N-SYN). In order to analyze the PDC dynamics we simplify the PDC into a piecewise constant (PWC) model that is well suited for precise analysis . Using the model we can clarify parameters condition for stable N-SYN in continuous conduction mode (CCM) and hyperchaos. The N-SYN in CCM is suitable to realize current sharing with lower ripple. Adjusting parameters including clock period, stable N-SYN in CCM is always possible. Presenting a simple test circuit, typical phenomena can be confirmed experimentally. These results provide basic information to design efficient PDCs and to develop nonlinear dynamical systems theory.

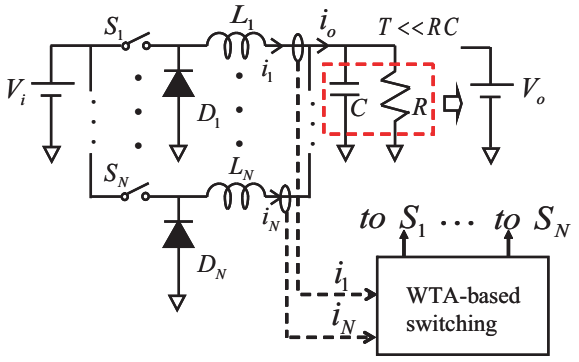

Figure 1: Paralleled buck converters.

2. Paralleled Buck Converters

Fig. 1 shows the PDC consisting of N buck converters ($N \geq 2$) that share the output current: $i_o \equiv \sum_{j=1}^{N} i_j$. The j-th converter has a switch S_j and a diode D_j which can be either of the three states:

State 1: S_j = ON , D_j = OFF and $0 < i$
State 2: S_j = OFF , D_j = ON and $0 < i$
State 3: S_j and D_j = OFF and $i = 0$

We then present two kinds of switching strategy.

Strategy 1 (Fig. 2 (a)):

State 1 → State 2 if $i_j = J_+$
State 2 → State 3 if $i_j = 0$
State 2 or State 3 → State 1 if i_j = min at $t = nT$

where J_+ is a upper threshold current and T is a clock period. The dynamic WTA is used in switching to State 1: if i_j is the minimum among i_1 to i_N at $t = nT$ then S_j is closed for $nT \leq t < (n+1)T$ regardless of past situation of S_j. We refer to the minimum i_j as the winner at $t = nT$. Note that the N converters are connected through the WTA-switching. Plural winners are possible only on State 3 where $i_j(nT) = 0$ must be minimum. If some converter operates to (not to) include State 3, it is said to operate in DCM (CCM).

Strategy 2 (Fig. 2 (b)):

State 2 → State 1 if $i_j = J_- \geq 0$
State 1 → State 2 if i_j = max at $t = nT$

where J_- is a lower threshold current. The dynamic WTA is used in switching to State 2: if i_j is the maximum among i_1 to i_N at $t = nT$ then S_j is opened for

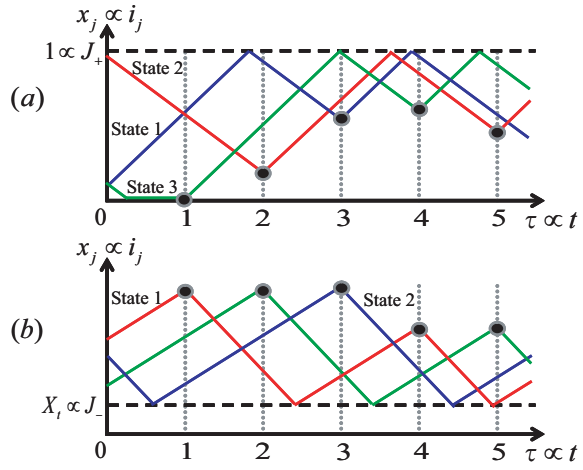

Figure 2: Switching rules. (a) Strategy 1. (b) Strategy 2.

$nT \le t < (n+1)T$ regardless of past situation of S_j. We refer to the maximum i_j as the winner at $t = nT$.

For simplicity we assume $RC >> T$ and replace the load with a constant voltage source V_o that is smaller than V_i. We also assume that the diode is ideal, all other circuit elements are ideal and $L_j = L$. The circuit dynamics for each state is described by Eq. (1).

$$L\frac{d}{dt}i_j = \begin{cases} V_i - V_o & \text{for State 1} \\ -V_o & \text{for State 2} \\ 0 & \text{for State 3} \end{cases} \tag{1}$$

Using the dimensionless variables and parameters:

$$\tau = \frac{t}{T},\ x_j = \frac{i_j}{J_+}$$
$$a = \frac{T}{LJ_+}(V_i - V_o),\ b = \frac{T}{LJ_+}V_o,\ X_t = \frac{J_-}{J_+} \tag{2}$$

the circuit dynamics is normalized into Eq. (3).

$$\frac{d}{d\tau}x_j = \begin{cases} a & \text{for State 1} \\ -b & \text{for State 2} \\ 0 & \text{for State 3} \end{cases} \tag{3}$$

Strategy 1:
State 1 $\rightarrow$ State 2 if $x_j = 1$
State 2 $\rightarrow$ State 3 if $x_j = 0$
State 2 or State 3 $\rightarrow$ State 1 if $x_j = \min$ *at* $\tau = n$

Strategy 2:
State 2 $\rightarrow$ State 1 if $x_j = X_t$
State 1 $\rightarrow$ State 2 if $x_j = \max$ *at* $\tau = n$

Note that the original parameters are integrated into three dimensionless parameters a, b and X_t.

In order to consider dynamics of the PDC, let us recall basic definitions in [6].

Let $\boldsymbol{x} = (x_1, \cdots, x_N)$. The PDC is said to exhibit N-SYN if Eq. (3) has periodic solution with period N such that

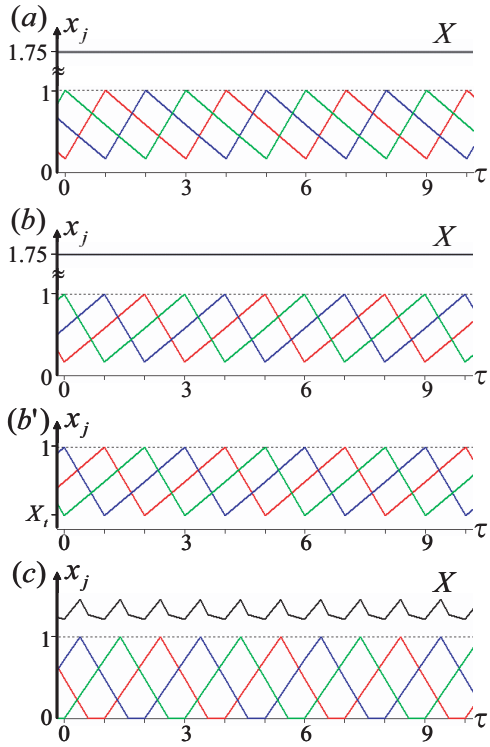

Figure 3: Typical waveforms ($N = 3$). Red, blue, green and black waveforms denote x_1, x_2, x_3 and X, respectively. (a) Stable 3-SYN in CCM by Strategy 1 for $(a^{-1}, b^{-1}) = (1.2, 2.4)$ and $R_p = 0$. (b) Unstable 3-SYN in CCM by Strategy 1 for $(a^{-1}, b^{-1}) = (2.4, 1.2)$ and $R_p = 0$. (b') Stable 3-SYN in CCM by Strategy 2 for $X_t = 0.167$. a^{-1}, b^{-1} and $R_p = 0$ are the same as (b). (c) Stable 3-SYN in DCM by Strategy 1 for $(a^{-1}, b^{-1}) = (1.4, 1.2)$ and $R_p = 0.238$.

$\boldsymbol{x}(\tau + N) = \boldsymbol{x}(\tau)$ and each cell becomes winner once during one period $0 \le \tau < N$.

Let $\boldsymbol{x_p} = (x_{p1}, \cdots, x_{pN})$ be a solution of N-SYN. The N-SYN is said to be stable for initial state if $\boldsymbol{x}(\tau)$ converges on $\boldsymbol{x}_p(\tau)$ as time goes for $\boldsymbol{x}(0) = \boldsymbol{x}_p(0) + \boldsymbol{\epsilon}(0)$ where $\boldsymbol{\epsilon}(0)$ is a small initial perturbation.

For a periodic solution with period M, $\boldsymbol{x}(\tau + M) = \boldsymbol{x}(\tau)$, ripple factor is given by $R_p = \max X(\tau) - \min X(\tau)$, where $0 \le \tau < M$, $X(\tau) \equiv \sum_{j=1}^{N} x_j(\tau)$ is the dimensionless output current.

Fig. 3 (a) and (b) show stable 3-SYN and unstable 3-SYN in CCM with low ripple in Strategy 1. We can not observe unstable N-SYN but chaotic behavior. Applying Strategy 2 to this unstable N-SYN, it changed to be stable as shown in Fig. 3 (b'). Fig. 3 (c) shows DCM operation. In general, DCM operation has higher ripple than CCM operation. For existence and stability of N-SYN we have the following results.

Proposition 1: In Strategy 2, N-SYN in CCM exists for all a and b. If $a < b$ then the N-SYN is stable. If $a > b$ then the N-SYN is unstable. The apex $X_{max} = 1$ is realized if $X_t = 1 - \frac{N}{a^{-1}+b^{-1}} \ge 0$.

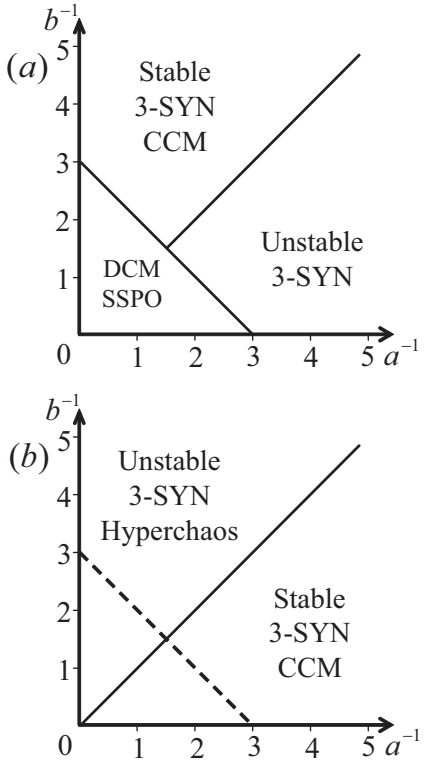

Figure 4: Existence and stability of N-SYN. (a) Parameter condition for $N = 3$ in Strategy 2. (b) Parameter condition for $N = 3$ in Strategy 1.

Proposition 2: In Strategy 1, N-SYN in CCM exists for $N < a^{-1}+b^{-1}$. The N-SYN is stable if $a > b$ and is unstable if $a < b$. The system operates in DCM for $N > a^{-1} + b^{-1}$

Fig. 4 shows the parameters condition for $N = 3$. As suggested in Fig. 3, the PDC of stable N-SYN in CCM has lower ripple factor than other modes. In order to realize stable N-SYN in CCM, $a^{-1} + b^{-1}$ should exceed N. Referring to Eq. (2), we obtain

$$a^{-1} + b^{-1} = \frac{LJ_+}{T}\frac{V_i}{V_o(V_i - V_o)} \tag{4}$$

That is, adjusting T and/or J_+ and/or L, the stable N-SYN in CCM can be achieved. Proofs of these results will be discussed in the developed version.

3. Experiments

We have fabricated a test circuit of the PWC model of WTA-based paralleled buck converters as shown in Fig. 5 (a). After current-to-voltage conversion (IVC) the node voltage v_{dj} is applied to the comparator and WTA circuit. The WTA circuit is realized using digital elements as shown in Fig. 5 (b). In this circuit, each node voltage v_{dj} is compared by the comparator and this circuit determines a term of the winner for each converter. Outputs of the WTA circuit are sampled with period T and applied to

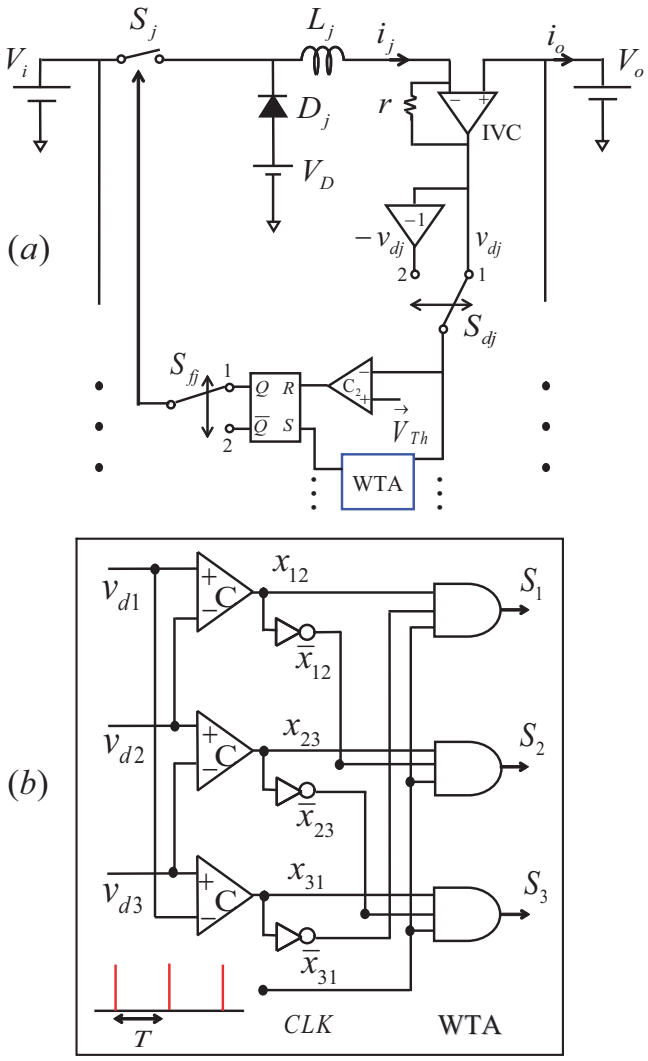

Figure 5: (a) Test circuit of paralleled buck converter where $v_{dj} = V_o - ri_j$. (b) WTA circuit: 071 (IVC), LM339 (comparator), 4066 (switch), 4013 (Flip-Flop), 4049 (Inverting Converter), 4082 (AND Gate).

set terminal of the flip-flops. Outputs of the comparator C_2 are applied to reset terminal. Outputs of the flip-flops control the switches S_1 to S_N. Switching between Strategy 1 and Strategy 2 are realized easily by switches S_{dj} and S_{fj}: connecting S_{dj} and S_{fj} to terminal 1 (terminal 2), Strategy 1 (Strategy 2) is realized.

Fig. 6 shows observed waveforms of the test circuit for $N = 3$ where we can see that stable 3-SYN in CCM with lower ripple can be confirmed in both Strategy 1 and 2. Note that stable 3-SYN in Strategy 2 of (b') is changed from chaotic behavior of (b) in which unstable 3-SYN is embedded (corresponding to Fig. 3 (b)).

4. Conclusions

We have presented the PDCs that can be realized N-SYN and ripple reduction for wide parameters region. Parameters condition for existence and stability of N-SYN is shown. Presenting a test circuit, typical behavior is confirmed experimentally. Future problems include analysis of bifurcation phenomena, design of practical circuits and experiments of them.

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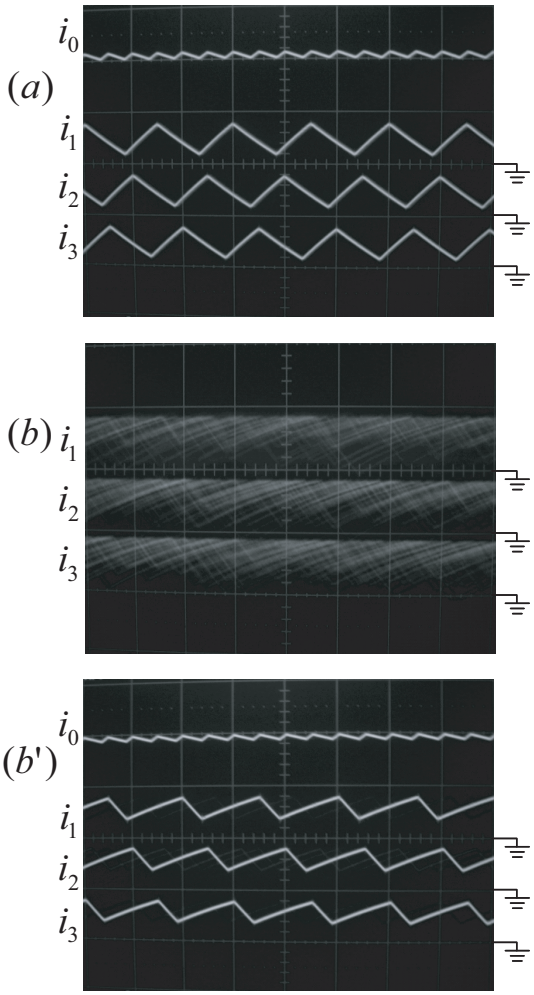

Figure 6: Observed waveforms of PWC model of paralleled buck converters for $N = 3$, $L \doteq 100$[mA] and $r \doteq 1$[kΩ]. Horizontal: 0.2ms/div, Vertical: 5mA/div. (a) 3-SYN in CCM for $(a^{-1}, b^{-1}) = (1.37, 4.33)$. $V_i \doteq 3.75$[V], $V_o \doteq 0.90$[V], $V_{Th} \doteq -3.00$[V], $T \doteq 0.10$[ms], $J_+ \doteq 3.90$[mA]. (b) Hyperchaos for $(a^{-1}, b^{-1}) = (3.34, 2.61)$. $V_i \doteq 3.33$[V], $V_o \doteq 1.87$[V], $V_{Th} \doteq -3.0$[V], $T \doteq 0.1$[ms], $J_+ \doteq 4.87$[mA]. (b') 3-SYN in CCM for $(a^{-1}, b^{-1}) = (3.34, 2.61)$. $V_i \doteq 3.33$[V], $V_o \doteq 1.87$[V], $V_{Th} \doteq 0$[V], $T \doteq 0.1$[ms].