The Effect of Via Spacing on the Signal Integrity Performance of PCB with Slotted Ground

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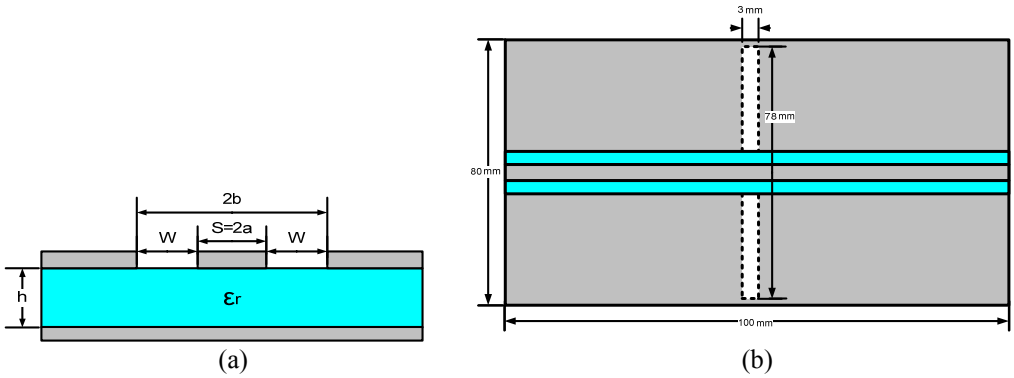
1. Introduction

Recently, there has been growing interest in the effect of slotted ground plane structures on the SI performance of PCBs. It is common to create slots in power/ground planes in high-speed printed circuit board (PCB) designs. In mixed signal circuits, split power/ground planes can isolate a noisy digital circuit from a sensitive analog circuit. Slots in the power/ground planes are also employed in PCBs with multiple power supplies in order to provide the DC isolation among different supplies[1]. However, slotted ground planes can give rise to electromagnetic interference (EMI) and distortion of original signals because a slot in a conducting plane can generate unwanted radiation that can easily couple to nearby signal traces. The slot can also pick up undesired energy from the surrounding circuits and couple this energy into the signal traces that cross over them. Moreover, in some packaging, it may not be possible to avoid routing signal traces over slotted ground plane because of strict space requirements[2].

In this paper, the effect of via spacing on the signal integrity of PCB with a slotted ground is investigated using Finite-Difference Time-Domain (FDTD) method based CST Ver. 2010[3]. For this purpose, via spacing and number of via around slotted ground are used as parameters for performance analysis. The signal integrity performance of FR4 PCB microstrip line through slotted ground with and without optimized via structure is evaluated. Test boards are fabricated and S-parameter and eye-diagram characteristics are measured to validate the effectiveness of the optimized via structure for signal integrity improvement.

2. PCB test board with slotted ground plane under study

The geometry of PCB test board under study is illustrated in figure 1. The proposed geometry consists of a signal line, the top ground, the bottom ground with slot, and an FR4 substrate. A signal line of width S and top grounds are separated by the spacing of W. An FR4 laminate (ε_r = 4.4, tanδ = 0.02, and size 89 mm × 100 mm × 1.6 mm) is used as a substrate. W is chosen to be 2.114mm which yields the characteristic impedance of 50 Ω. The length of the signal line is 80 mm. The size of the slot on the bottom ground is 30 mm × 78 mm. The designed structure can be used as a conductor backed coplanar waveguide (CBCPW) from 0 to 5 GHz.



(a) (b)

Figure 1: Geometry of PCB test board with slotted ground for analysis: (a) Side View, (b) Top View

3. The effect of loading of vias

The top ground planes are connected to the bottom ground plane through a number of through-vias of radius R with via spacing A, and the via radius is chosen to be 0.35 mm. The effect of loading of vias along a signal line is examined.

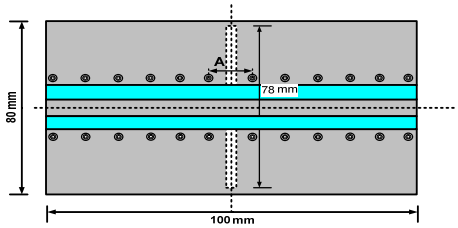
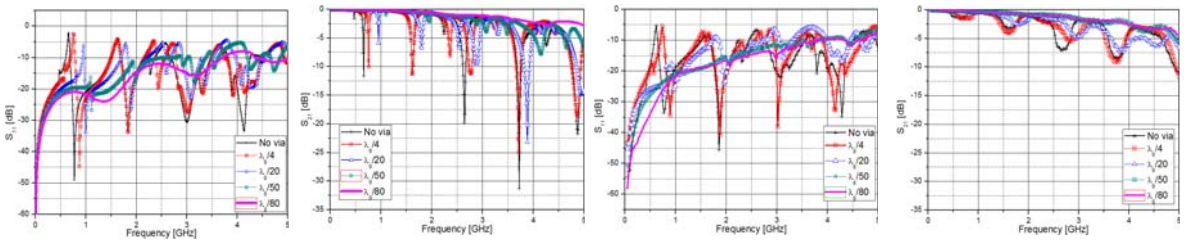


Figure 2: Geometry of PCB test board with slotted ground and vias for analysis

S-parameter characteristics for different via spacing (A) value are analyzed and are illustrated in figure 3. The slotted ground without vias causes undesired resonances since it acts as an antenna. However, as the value of the via spacing decreases (or number of via holes increases), the undesired resonances form the PCB are eliminated.

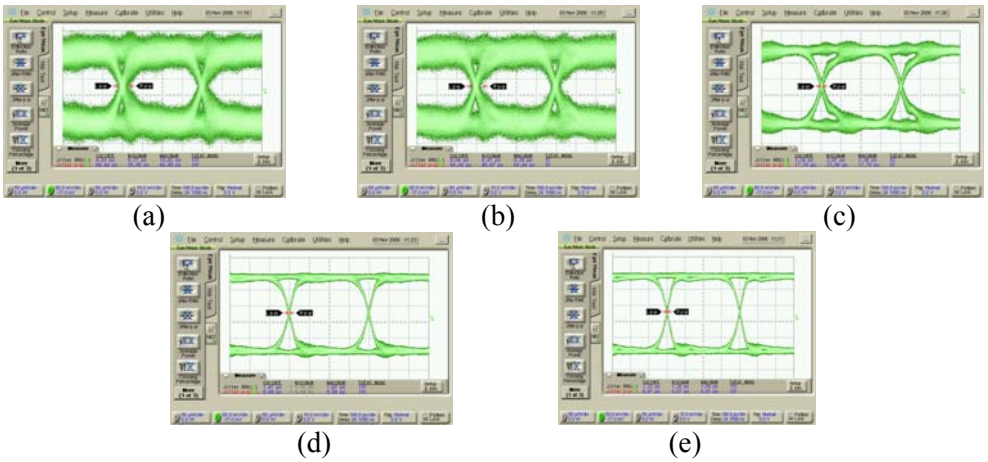


(a) (b) (c) (d)

Figure 3: S-parameters for various via spacing value for slotted ground: (a) Simulated return loss (S_{11}), (b) Simulated transfer characteristics (S_{21}), (c) Measured return loss (S_{11}), (d) Measured transfer characteristics (S_{21}).

The results show that the transfer characteristic for via spacing A = $\lambda_g/80$ yields the best performance over the frequency band of interest. It is observed both from simulation and measurement that the value of via spacing determines the resonances.

In order to investigate the effect of via spacing in time domain, eye-diagrams are measured. Figure 4 shows the measured eye diagrams when PRBS(Pseudo Random Binary Sequence) is applied to the interconnection.



(a) (b) (c)

(d) (e)

Figure 4: Eye diagram results for different via spacing value: (a) **N**o vias, (b) $\lambda_g/4$ (c) $\lambda_g/20$ (d) $\lambda_g/50$ (e) $\lambda_g/80$.

Table 1: Performance comparison of geometry shown in Figure 2

	Noise margin (%)	Max. distortion (%)	Jitter (%)
No vias	34	13	9.6
$\lambda_g/4$	40	16	10
$\lambda_g/20$	80	30	37
$\lambda_g/50$	91	75	75
$\lambda_g/80$	97	90	97

From figure 4 and table 1, it is observed that the proper choice of via spacing can also improve jitter, maximum distortion and noise margin characteristics in time domain analysis as expected from the frequency domain results. According to the eye diagram measurement, the λg/80 case also has the best performance among no via, λg/4, λg/20, and λg/50 cases.

In order to investigate the effect of via spacing on the unnecessary radiation suppression, radiation patterns of the PCB test board are measured. Figure 5 shows the coordinate system of the PCB test board for radiation pattern measurement in anechoic chamber. A 50 Ω terminator is used for the measurement at port 2.

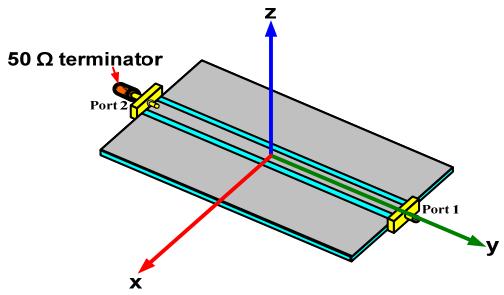


Figure 5: Coordinate system of the PCB test board for radiation pattern measurement.

Figure 6 ~ 7 show measured radiation patterns for different via spacings on PCB with slotted ground at 1.7 GHz and 2.3 GHz, respectively.

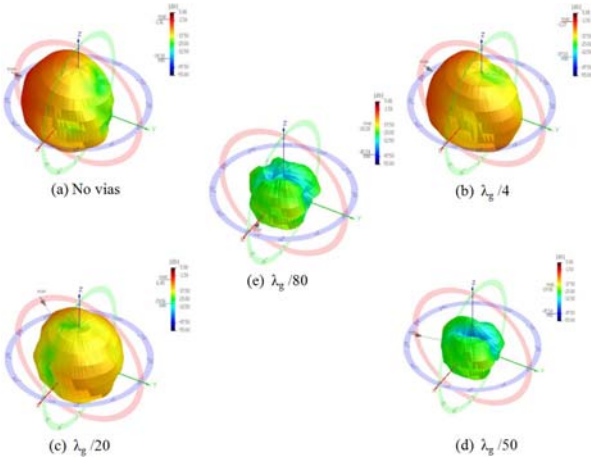


Figure 6: Measured radiation patterns for different via spacing on PCB with slotted ground at 1.7 GHz: : (a) **N**o vias, (b) $\lambda_g/4$ (c) $\lambda_g/20$ (d) $\lambda_g/50$ (e) $\lambda_g/80$.

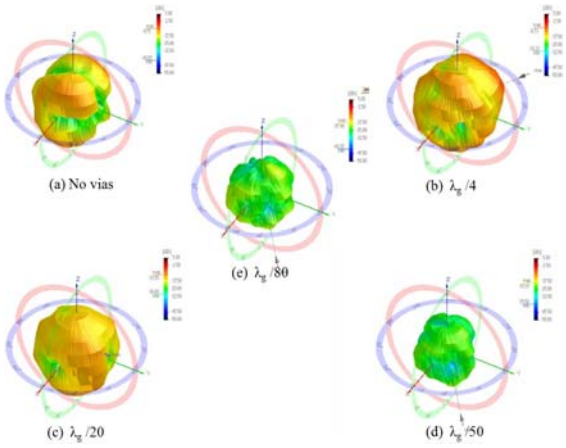


Figure 7: Measured radiation patterns for different via spacing on PCB with slotted ground at 2.3 GHz: : (a) **N**o vias, (b) $\lambda_g/4$ (c) $\lambda_g/20$ (d) $\lambda_g/50$ (e) $\lambda_g/80$.

Form measured result, the suppression effect of via spacing on unwanted radiation from PCB board is very clear for all frequencies.

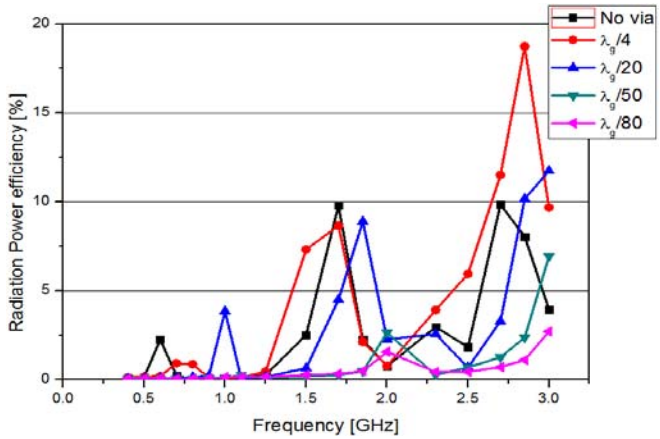


Figure 8: Measured radiation power efficiencies for different via spacings on PCB with slotted ground.

The measured radiation power efficiency shown in Figure 8 clearly reveals that the smaller the via spacing is, the lower the radiation power efficiency is. Therefore, via spacing can improve the transfer characteristic, signal integrity as well as unnecessary radiation in PCB with slotted ground.

4. Conclusion

The effect of via spacing on the signal integrity is analyzed. From the measured results, it is observed that the proper choice of via spacing improves jitter, maximum distortion and noise margin characteristics as well as reduces unnecessary radiation

Acknowledgments

This research was supported by a grant(07교통체계-미래02) from Transportation System Innovation Program funded by MLTM (Ministry of Land, Transport and Maritime Affairs).

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