An Analysis of Second-Order Sigma-Delta Modulator and its Application to AC Load Monitor

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Abstract—We analyzed the behavior of discrete-time second-order sigma-delta modulators in state-space. As a result of the analysis it is found that the sigma-delta modulated signals never contain a certain sub-sequence set which changes depending on the polarity of the inputs to the sigma-delta modulator. Thus, by detecting the sub-sequences we can determine whether the input is positive or negative. We applied the sub-sequence detection to the measurement of average current and power factor for linear AC circuits with sinusoidal power sources. The error of the power factor measurement is less than 0.1.

1. Introduction

Sigma-delta (SD) modulation [1] is a very popular technique for analog-to-digital and digital-to-analog conversion. The converters based on SD modulation have been used not only in audio signal processing but also in high-frequency communication signal processing.

Piecewise linear circuits are widely used in signal processing and communication fields. Piecewise linear operators on first-order SD modulated binary signals have been proposed [2]. The operation exploits a characteristic of the signals. The characteristic is that the signal sequence does not contain a sub-sequence $\{-1, -1\}/\{+1, +1\}$ when the input to the SD modulator is positive/negative.

Sub-sequences which reflect polarity of the inputs to second and higher-order SD modulators have not been reported although these modulators have been investigated [3]. In this paper we analyze the behavior of second-order SD modulators in state-space to search for the sub-sequences and apply the sub-sequence detection to AC load monitoring.

2. Second-Order Sigma-Delta Modulator

Figure 1 shows a discrete-time second-order SD modulator with a 2-level quantizer. Let $x(n)$, $u(n)$ and $y(n)$=sgn($u(n)$) be an input, the state of integrator INT2 and the binary output of the modulator. Index n denotes time step. The behavior of the modulator is governed

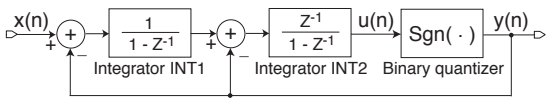

Figure 1: The second-order SD modulator.

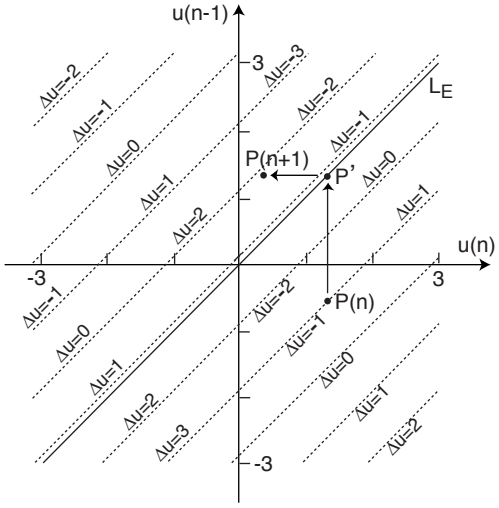

Figure 2: The values that $\Delta_u(n+1)$ takes in state-space $u(n)$−$u(n-1)$.

by the following difference equation possessing a piecewise constant term p_c:

$$u(n+1) - 2u(n) + u(n-1) = x(n) + p_c(n) \tag{1}$$

$$\begin{aligned} p_c(n) &= -2\mathrm{sgn}(u(n)) + \mathrm{sgn}(u(n-1)) \\ &= \begin{cases} -1 & \text{if } (u(n), u(n-1)) \in Q_I \\ 3 & \text{if } (u(n), u(n-1)) \in Q_{II} \\ 1 & \text{if } (u(n), u(n-1)) \in Q_{III} \\ -3 & \text{if } (u(n), u(n-1)) \in Q_{IV} \end{cases} \end{aligned}$$

where Q_I, Q_{II}, Q_{III} and Q_{IV} denote the first, second, third and fourth quadrants of state-space $u(n)$−$u(n-1)$.

We define a difference $\Delta_u(n)$ of the state as

$$\Delta_u(n) = u(n) - u(n-1) \tag{2}$$

Then, Eq. (1) is transformed to

$$\Delta_u(n+1) = \Delta_u(n) + x(n) + p_c(n) \tag{3}$$

Figure 2 shows the values that $\Delta_u(n+1)$ takes in the state-space when the input is a small DC signal, $x(n)$=ϵ. The trajectory of $P(n)$=($u(n)$, $u(n-1)$) on the state-space can be obtained easily by the following procedure: Memorize $\Delta_u(n+1)$ at $P(n)$. Move point P vertically and stop it on line L_E:$u(n)$−$u(n-1)$= 0. Then, vertical coordinate of $P(n+1)$ is determined. Let a point on Line L_E at

which $P(n)$ was moved be $P'(n)$. Recall $\Delta_u(n+1)$ and move $P'(n)$ horizontally by $\Delta_u(n+1)$. Then, horizontal coordinate $u(n+1)$ of $P(n+1)$ is determined.

3. Behavior of the Modulator

We investigate the motion of point P when small positive DC input, $x(n)=\epsilon>0$, is given to the SD modulator. We first consider the motion of P starting at a point in $A\cup B\subset Q_{II}$ shown in Fig. 3(a). As we will see later in Figs. 3(b) and (e), the point P always gets in area $A\cup B$ when it returns to Q_{II}. Then, the investigation below will deal with all the states that the SD modulator can take.

Area B is divided into four sub-areas B_I, B_{II}, B_{III} and B_{IV}, as shown in Fig. 3(b). Points P in B move as follows:

(i) If $P(n)\in B_I$, $P(n+1)\in B_{I+}\subset Q_{IV}$ and $P(n+2)\in A_{II}\subset A$.

(ii) If $P(n)\in B_{II}$, $P(n+1)\in B_{II+}\subset Q_{IV}$, $P(n+2)\in B_{II}$, $\cdots$, $P(n+m-1)\in B_{II+}$, $P(n+m)\in B_I$, m: even integer. After time $n+m$, point P moves as mentioned in (i).

(iii) If $P(n)\in B_{III}$, $P(n+1)\in B_{III+}\subset Q_{IV}$, $P(n+2)\in B_{III}$, $\cdots$, $P(n+m-1)\in B_{III+}$, $P(n+m)\in B_{IV}$, m: even integer. After time $n+m$, point P moves as will be mentioned in (iv).

(iv) If $P(n)\in B_{IV}$, $P(n+1)\in B_{IV+}\subset Q_{IV}$ and $P(n+2)\in Q_I$.

Detailed analysis derives that area $B_{I+}\cup B_{II+}$ is given by the following expression. For a small real value ϵ, there exists an integer N, and

$$\begin{aligned} & B_{I+}\cup B_{II+} \qquad (4)\\ &= \bigcup_{n=0}^{N}\{(u(n),u(n-1))|u(n)\geq 0,\ u(n-1)<0,\\ &\qquad u(n-1)\geq \frac{3+2n}{2+2n}u(n)-\frac{3-(2n+3)\epsilon}{2}\Big\} \end{aligned}$$

Points P in A move as shown in Fig. 3(c), if $P(n)\in A$, then $P(n+1)\in A_+$ and $P(n+2)\in A_{2+}$. A more detailed observation on the motion is as follows: Area A contains a sub-area A_I.

(v) If $P(n)$ is in difference set $A-A_I$, $P(n+1)$, $\cdots$, $P(n+m-1)\in Q_{III}$, $P(n+m)\in(Q_{IV}-B_{I+}\cup B_{II+})$, $P(n+m+1)$, $\cdots$, $P(n+m+m'-1)\in B_{III}\cup B_{IV}\cup B_{III+}\cup B_{IV+}$, and $P(n+m+m')\in Q_I$, where $2\leq m\leq 3$, $1\leq m'$.

(vi) If $P(n)\in A_I$, $P(n+1)\in A_{I+}\subset Q_{III}$, $P(n+2)\in A_{I2+}\subset B_{I+}\cup B_{II+}$, $P(n+3)\cdots$, $P(n+3+m-1)\in B_I\cup B_{II}\cup B_{I+}\cup B_{II+}$, and $P(n+3+m)\in A_{II}\subset A$, where $m\geq 0$.

Next, we consider the motion of P starting at a point in $C\cup D\subset Q_{IV}$ shown in Fig. 3(e). All the points $P(n)$ which are in $A\cup B$ and will not return to A_{II} will certainly be in $C\cup D$. Area D is a subset of B_{IV+}, $D\subset B_{IV+}$. Points P in $C\cup D$ move as follows:

(vii) If $P(n)\in C\cup D$, $P(n+1)\in C_+\cup D_+\subset Q_I$ and $P(n+2)\in C_{2+}\cup D_{2+}$. Points $P(n+2)\in(C_{2+}\cup D_{2+})\cap Q_I$ move to $P(n+3)\in C_{3+}\cup D_{3+}$. Points $P(n+3)\in(C_{3+}\cup D_{3+})\cap Q_I$ move to $P(n+4)\in C_{4+}\cup D_{4+}$.

Then, from (i)$-$(vii) we find that point P started at any point in $A\cup B$ never gets into $Q_{II}-A\cup B$ when it returns to Q_{II}.

When $\epsilon>0$, $A_I\cap A_{II}=\phi$ and $A_I\cap(C_{+k}\cup D_{+k})=\phi$, k=2,3 and 4, as Figs. 3(c) and (e) show, which means that $P(n)\notin A_I$ when the SD modulator is in steady-state. Then, we obtain

(viii) The stationary trajectory of $P(n)$ never contains the following path: $P(n)\in Q_{III}$, $P(n+1)$, ..., $P(n+m)\in Q_{II}\cup Q_{IV}$, $P(n+m+1)\in Q_{III}$, where, $m\geq 2$.

When $\epsilon<0$, $A_I\cap A_{II}\neq\phi$ and $A_I\cap(C_{+k}\cup D_{+k})\neq\phi$, as shown in Figs. 3(d) and (f). Thus, the stationary trajectory of $P(n)$ may contain the path in (viii).

We define a ternary sequence $\{z(n)\}$ as

$$\begin{aligned} z(n) &= y(n)+y(n-1)=\mathrm{sign}(u(n))+\mathrm{sign}(u(n-1))\\ &= \begin{cases} 2 & \text{if } (u(n),u(n-1))\in Q_I\\ 0 & \text{if } (u(n),u(n-1))\in Q_{II}\cup Q_{IV}\\ -2 & \text{if } (u(n),u(n-1))\in Q_{III}\end{cases} \qquad (5)\end{aligned}$$

and two sub-sequences S_+, S_- as

$$\begin{aligned} S_+ &= \{+2,0,...,0,+2\}\\ S_- &= \{-2,0,...,0,-2\}\end{aligned} \qquad (6)$$

The sub-sequences contain at least two "0"s and no "$\mp$2" between "$\pm$2". The above investigation into the behavior of the second-order SD modulator implies that sequence $\{z(n)\}$ has the following property:

Property 1:

Input $x(n)$ to the second-order SD modulator is non-positive if $S_-\subset\{z(n)\}$. $x(n)$ is non-negative if $S_+\subset\{z(n)\}$.

The first half of the property is the contraposition to the result (viii) of the investigation. The last half of the property is derived by a similar investigation for $x(n)=\epsilon<0$.

4. Application to AC load Monitor

Property 1 directs that we can determine whether the input to second-order SD modulator is positive or negative by detecting sub-sequences S_+ and S_-. In this section we apply the sub-sequence detection to the measurement of average voltage, average current and power factor for AC circuits. We assume that truly sinusoidal AC power source is connected to a linear load. Thus, the waveforms of the voltage and the current through the load are considered to be truly sinusoidal and expressed by

$$\begin{aligned} V(t) &= A_V cos(2\pi t/T)\\ I(t) &= A_I cos(2\pi t/T+\theta)\end{aligned} \qquad (7)$$

Inputs to the measurement circuits are binary sequences $V_{SD}(n)$, $I_{SD}(n)$ obtained by modulating $V(t)$ and $I(t)$ with the second-order SD modulators shown in Fig. 1.

A circuit to measure average values of the AC voltage and current is shown in Fig. 4(a). A circuit in a dotted square in the figure detects the sub-sequences. It sets and resets a SR flip-flop when it detects S_+ and S_-. An up/down counter CNT1 integrates $V_{SD}(n)$, $I_{SD}(n)$ while $V(t)$ and $I(t)$ are non-negative. Assuming that the sub-sequence detection circuit sets and resets the SR flip-flop

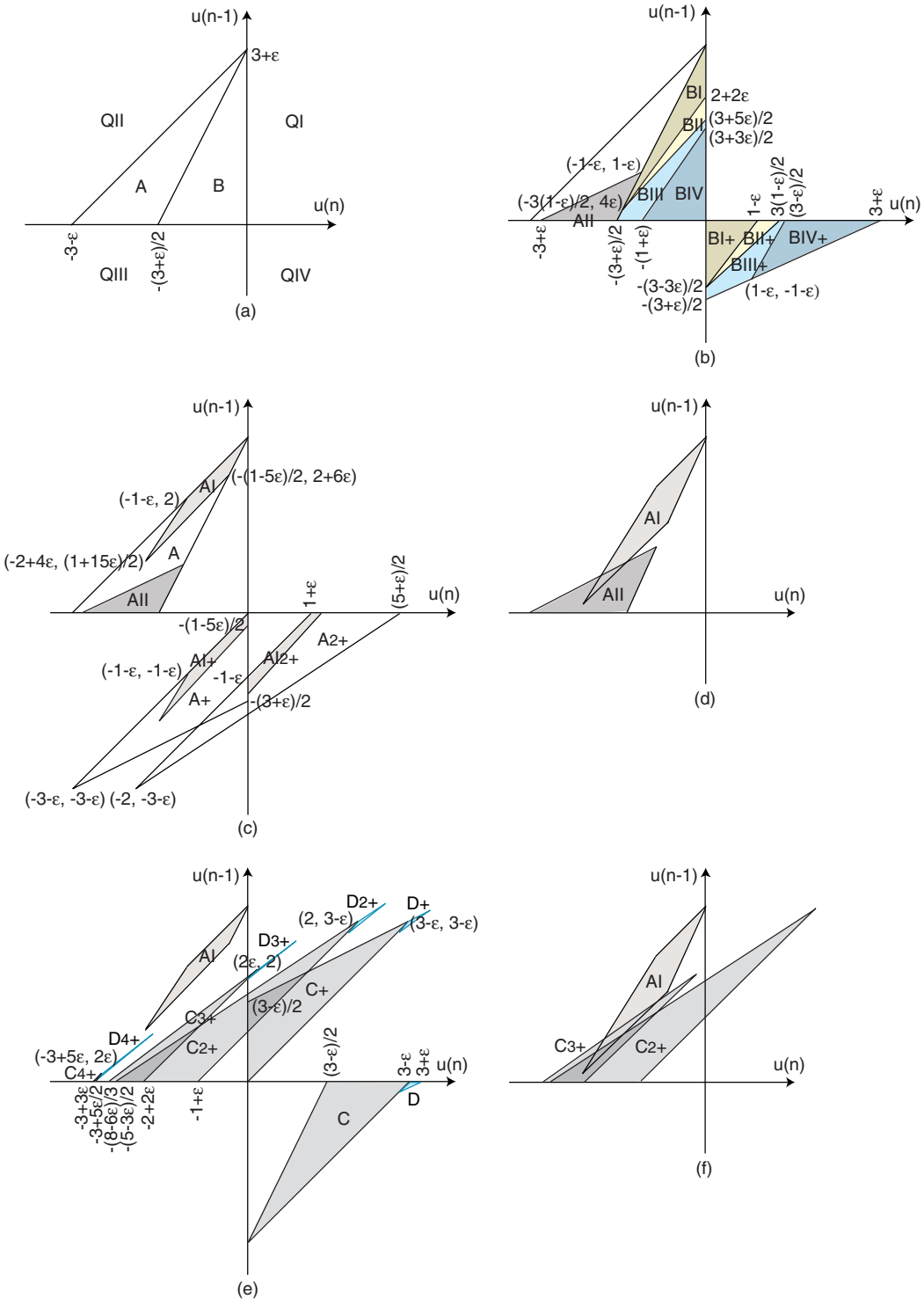

Figure 3: Behavior of the second-order SD modulator in state-space $u(n)-u(n-1)$.

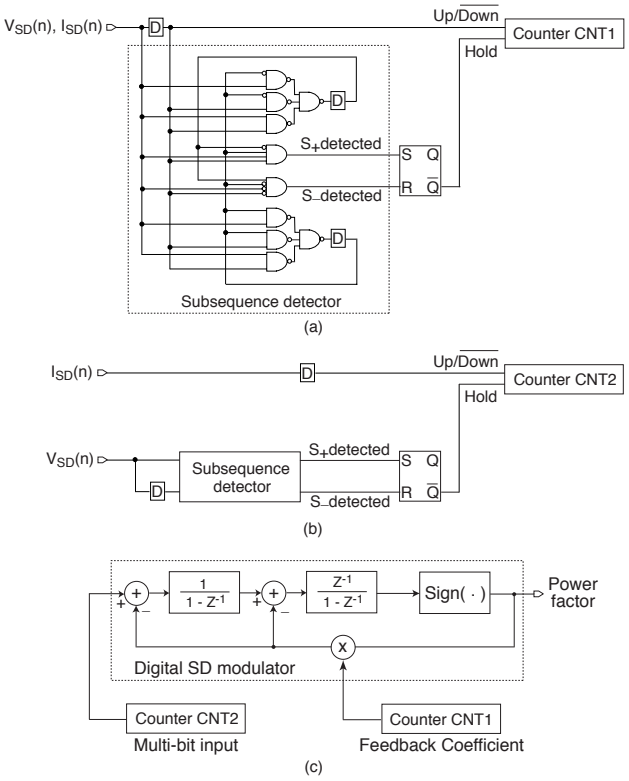

Figure 4: The circuits for average value and power factor measurement.

at the moment of $V(t)$ and $I(t)$ crossing zeros without any delay, we obtain in CNT1 their average values V_{avr}, I_{avr},

$$V_{avr} = \int_{-T/4}^{T/4} V(t)dt = \frac{TA_V}{\pi} \approx \sum_{n=-T/4}^{T/4} V_{SD}(n) \qquad (8)$$

$$I_{avr} = \int_{-T(\frac{1}{4}-\frac{\theta}{2\pi})}^{T(\frac{1}{4}-\frac{\theta}{2\pi})} I(t)dt = \frac{TA_I}{\pi} \approx \sum_{n=-T(\frac{1}{4}-\frac{\theta}{2\pi})}^{T(\frac{1}{4}-\frac{\theta}{2\pi})} I_{SD}(n) \qquad (9)$$

A circuit shown in Fig. 4(b) integrates $I_{SD}(n)$ while $V(t)$ is non-negative. Ideally we can obtain the following value in counter CNT2:

$$\begin{aligned} I_{avr}\cos\theta &= \int_{-T/4}^{T/4} I(t)dt = \frac{TA_I\cos\theta}{\pi} \\ &\approx \sum_{n=-T/4}^{T/4} I_{SD}(n) \end{aligned} \qquad (10)$$

Figure 4(c) shows a circuit for power factor computation. We obtain power factor $\cos\theta$ in bit-stream form from the output of a second-order digital SD modulator whose input and the feedback coefficient are the contents of CNT2 and CNT1, namely $I_{avr}\cos\theta$ and I_{avr}.

Results of the power factor measurement by using the circuits presented in Fig. 4 are shown in Tab. 1. We found experimentally that the SD modulators delay in generating subsequences after their inputs cross zero. Small measurement errors shown in Tab. 1 are mainly due to the delay.

Table 1: Results of the power factor measurement.

Amplitude A_V	Amplitude A_I	Period (xTs)	Phase θ	Obtained power factor	Error
0.6	0.1	2^{12}	π/6	0.86	0.006
			π/4	0.70	0.007
			π/2	0.10	0.100
		2^{16}	π/6	0.86	0.006
			π/4	0.70	0.007
			π/2	0.02	0.020
	0.9	2^{12}	π/6	0.82	0.046
			π/4	0.66	0.047
			π/2	0.10	0.100
		2^{16}	π/6	0.86	0.006
			π/4	0.70	0.007
			π/2	0.02	0.020

Input range of SD modulators: -1< V(n), I(n) < +1
Ts: Sampling interval
Resolution of power factor: 0.02
Error: |obtained power factor - cosθ|

5. Conclusions

We have analyzed the behavior of second-order SD modulators in state-space. From the analysis we find that the SD modulated signals never contain a certain sub-sequence set which changes depending on the polarity of the inputs to the SD modulator. We have applied the sub-sequence detection to the measurement of average current and power factor for linear AC circuits with sinusoidal power sources. The error of the power factor measurement is less than 10 percent.

Our future subjects include exploring characteristics of second and higher-order SD modulators with various loop filters which stabilize the modulation.

Acknowledgment

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