

An Ultra Low-Power High-Speed Rail-to-Rail Buffer Amplifier for LCD Source Drivers

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Abstract—An ultra low-power high-speed rail-to-rail buffer amplifier with improved current summing circuit is proposed for LCD source drivers. By placing two complementary differential pairs in parallel, it is possible to obtain a rail-to-rail input stage. Then, a current summing circuit with two embedded comparators is proposed. With the proposed current summing circuit, the output stages will be turned off at static state to reduce quiescent current, while keeping large driving capacity when they are turned on at dynamic state. In addition, the proposed buffer amplifier will not increase the chip size so that the buffer amplifier can be made compact. Simulation with a $0.35 \mu\text{m}$ CMOS technology demonstrates that the buffer has a quiescent current of $2.0 \mu\text{A}$ and a maximum tracking error of 0.16 LSB with 100% rail-to-rail input swing. Settling time of $1.5 \mu\text{s}$ and $2.1 \mu\text{s}$ for the rising and falling edge is measured for rail-to-rail voltage swing with 600 pF capacitance load, which is sufficient for driving large LCD panels.

I. INTRODUCTION

The block diagram of the source driver for Liquid Crystal Display (LCD) is depicted in Fig. 1 [1]. Usually it contains a shift register, inversion controller, input register, data latch, DACs and output buffers to drive each pixel. For the output buffers, first, large number of output buffers are needed. For example, in a UXGA panel, there are 1200×3 such buffers. As LCD is now being widely used on compact battery powered devices, size factor and power constrains becomes severe. Second, the load of Column drivers are storing capacitors and the capacitance of the liquid crystals. So it is expected to have high speed operation even under highly capacitive load. Third, since high color depth displaying is common today, output buffers should track the input signal with high accuracy. In a word, output buffers are essential in determining the performance of source drivers [2]. Therefore, building output buffers with compact size, low-power, high-speed and high accuracy at the same time becomes indispensable.

Many methods eliminating the quiescent current have been proposed. Yu et al [3] proposed a low-power buffer amplifier in which a comparator was incorporated in the feedback loop to reduce quiescent power. However, this circuit cannot work when input is near GND or VDD. Lu et al [4] proposed a high-speed driving scheme and a rail-to-rail buffer amplifier where two comparators are used to turn off the output stages at static state, and turn on them when transient. However, the newly added comparators will increase the size of the buffer and also consume some static current.

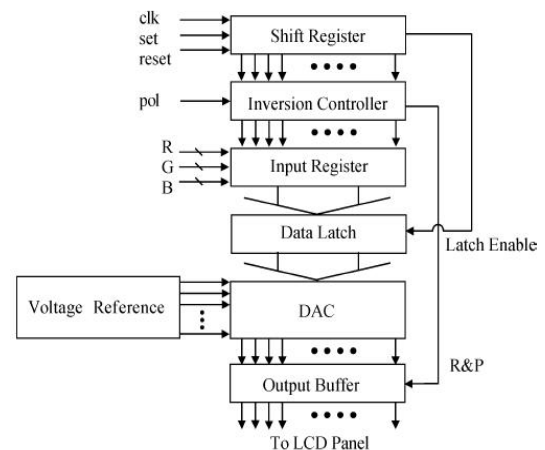


Fig. 1. Block diagram of source driver for LCD.

In this paper, a low-power, high-speed, rail-to-rail buffer amplifier with improved current summing circuit is proposed. By embedding two comparators in the current summing circuit, the switching of output stages can be achieved without extra area and power. The buffer has large driving capacity while drawing little quiescent current. In addition, it is of high accuracy and suitable to drive a wide range of capacitive load.

This paper is organized as follows. Architecture and simulation results of the proposed buffer amplifier are described in Sect. II. Comparison with existing works is discussed in Sect. III. The conclusions are described in Sect. IV.

II. PROPOSED BUFFER AMPLIFIER

In this section, the circuit implementation is described. Then the simulation results of the proposed buffer amplifier are demonstrated.

A. Circuit Implementation

The proposed buffer amplifier is shown in Fig. 2. The buffer amplifier incorporates the bias circuit (M1-M4), two rail-to-rail differential input stages (M6-M9), the current summing circuit (M11-M20) with embedded comparators (M14, M15, M17, M18) and two output stages (M21-M24). The input signal is applied to the non-inverting terminal (V_{in1}) and the output node of the first output stage is connected to the inverting terminal (V_{in2}) to form the unit-gain amplifier. A resistor is

put between two output nodes of the output stages. The sizes of resistors in the buffer amplifier are designed as

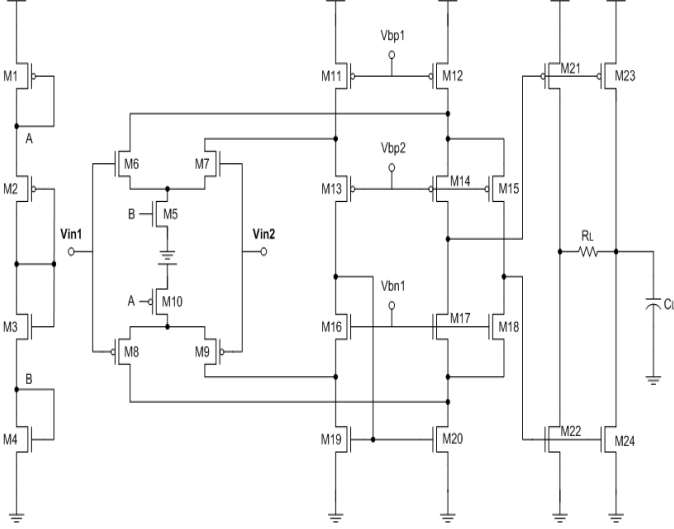


Fig. 2. Proposed buffer amplifier for LCD column driver.

$$\left(\frac{W}{L}\right)_5 = \left(\frac{W}{L}\right)_{10} = m, \quad (1)$$

$$\left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_8 = 1, \quad (2)$$

$$\left(\frac{W}{L}\right)_{14} = \frac{1}{2} \left(\frac{W}{L}\right)_{13} + \Delta \left(\frac{W}{L}\right), \quad (3)$$

$$\left(\frac{W}{L}\right)_{15} = \frac{1}{2} \left(\frac{W}{L}\right)_{13} - \Delta \left(\frac{W}{L}\right), \quad (4)$$

$$\left(\frac{W}{L}\right)_{17} = \frac{1}{2} \left(\frac{W}{L}\right)_{16} - \Delta \left(\frac{W}{L}\right), \quad (5)$$

$$\left(\frac{W}{L}\right)_{18} = \frac{1}{2} \left(\frac{W}{L}\right)_{16} + \Delta \left(\frac{W}{L}\right), \quad (6)$$

$$\left(\frac{W}{L}\right)_{13} = \left(\frac{W}{L}\right)_{16}, \quad (7)$$

and

$$\left(\frac{W}{L}\right)_{11} = \left(\frac{W}{L}\right)_{19} = 1. \quad (8)$$

Notice that from (8), the bias transistors M5 and M10 of the input differential pairs have the same aspect ratio over M4 and M1. So the total currents of input stages are the same. Joined with (2) and (6), current flows in M13 and M16 can be written as

$$I_{13} = I_{16} = I_{11} - \frac{m}{2} I_b, \quad (9)$$

where I_b refers to the bias current.

Since M14, M15 and M17, M18 share the same gate voltage respectively and have different aspect ratio, it is possible to make them work in different regions when at static state to

shut down the output stages. As M19 and M20 have the same gate voltage, the current of M13 and M16 will be mirrored to the right-hand side. For the aspect ratio of M14 and M18 is larger than that of M17 and M15, M14 and M18 will be pushed towards triode region and M17 and M15 in the saturate region. So the drain voltage of M14 is high and that of M15 is low. Thus, the gate of M21 and M23 will be near $V_{DD} - 2|V_{DSP}|$, where V_{DSP} represents drain-source voltage of p-type transistors. This will in turn close the p-type output transistors when the circuit is at static state. On the other hand, M22 and M24 will also be cutoff as a result of a gate voltage near $2V_{DSN}$, where V_{DSN} stands for drain-source voltage of n-type transistors.

Currents flow in the comparators can be expressed as

$$I_{14} = I_{17} = \left(I_{11} - \frac{m}{2} I_b\right) \times \frac{\left(\frac{W}{L}\right)_{17}}{\left(\frac{W}{L}\right)_{13}}, \quad (10)$$

$$I_{15} = I_{18} = \left(I_{11} - \frac{m}{2} I_b\right) \times \frac{\left(\frac{W}{L}\right)_{15}}{\left(\frac{W}{L}\right)_{13}}. \quad (11)$$

Therefore, the conditions for keeping the output stages off at static states are

$$\begin{aligned} V_{SG21} &= V_{SG23} = V_{SD12} + V_{SD14} \\ &\approx V_{SD12} + \frac{\left(I_{11} - \frac{m}{2} I_b\right) \times \frac{\left(\frac{W}{L}\right)_{17}}{\left(\frac{W}{L}\right)_{13}}}{\mu_p C_{ox} \left(\frac{W}{L}\right)_{14} (V_{SG14} - |V_{tp14}|)} \\ &< |V_{tp21}| \end{aligned} \quad (12)$$

and

$$\begin{aligned} V_{GS22} &= V_{GS24} = V_{DS20} + V_{DS18} \\ &\approx V_{DS20} + \frac{\left(I_{11} - \frac{m}{2} I_b\right) \times \frac{\left(\frac{W}{L}\right)_{15}}{\left(\frac{W}{L}\right)_{13}}}{\mu_n C_{ox} \left(\frac{W}{L}\right)_{14} (V_{GS18} - V_{tn18})} \\ &< V_{tn22}, \end{aligned} \quad (13)$$

where μ_p and μ_n represent the mobility in the p-type and n-type channels and C_{ox} is the gate oxide capacitance per unit area.

Despite the different output voltages of the embedded comparators, the current summing circuit, however, is balanced during the 0-VDD input range. The sum of the aspect ratio of M14, M15 and M17, M18 are equal to those of M13 and M16, respectively. As a result, the static currents in the left-hand and right-hand side are approximately the same.

Frequency compensation is realized by a resistor between two output nodes of the output stages, together with the load capacitance C_L . A zero will be formed at transient. Unlike conventional method for compensation of two-stage operational amplifier by using on-chip Miller capacitor [5], this methods will reduce the size of the buffer very much.

At dynamic state, when V_{Vin1} is decreased, drain voltages of M20 and M12 will be increased. since the gate of M14 and M18 are both fix biased, the gate voltages of M21-M24 will all increased. While p-type output transistors will be cutoff even more, n-type output transistors will be open to discharge the load capacitance. Actually, increasing the drain voltage

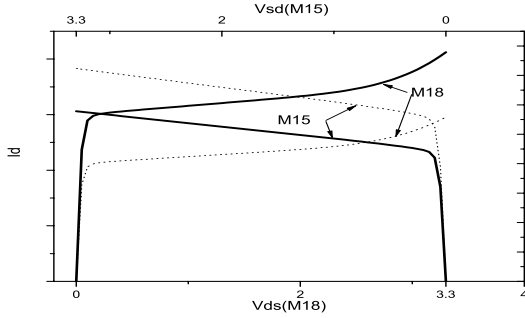


Fig. 3. I-V curves of M15 and M18.

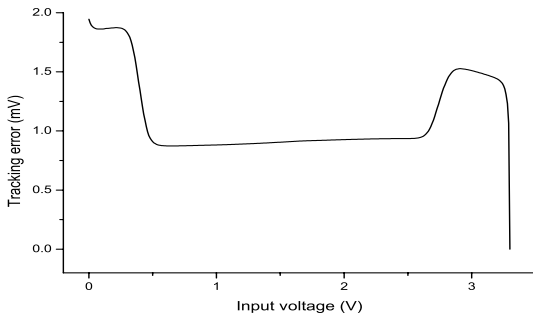


Fig. 4. Tracking error.

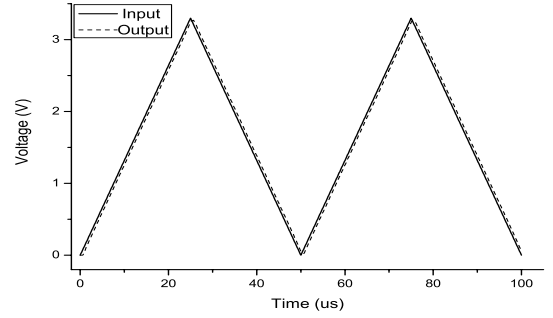


Fig. 5. 20 kHz, 3.3V triangular input response, 600 pF load capacitance.

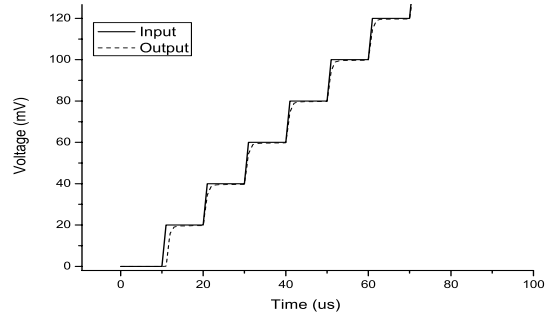


Fig. 6. Small scale step response.

of M18 (the gate voltage of M22 and M24 as well) moves the intersection point of the I-V curves in Fig. 3 rightward, resulting that the M15 will be in the triode region while M18 is in the saturation region, as the dashed line in the figure.

Similarly, when the input V_{Vin1} is increased, p-type output transistors M21 and M23 will be open to charge the load. The gate voltages of n-type and p-type output transistors can be sufficiently high/low to ensure a fast response, though not exactly VDD or GND. With the negative feed back from the connecting point of M21 and M22 to the inverting input terminal, when the input difference is near zero, the output stages will gradually be turned off. Analysis shows that the driving capacity doesn't depend on the biasing current, as in traditional buffers. Therefore, circuits other than the output stages can be made with small sizes [4].

B. Simulation Results

The buffer amplifier was realized in a 0.35 μm CMOS process. A maximum quiescent current of 2.0 μA is obtained at the supply voltage of 3.3 V. As mentioned, the output stages are off at static state so the proposed buffer amplifier consumes little quiescent power. DC transfer characteristics is analyzed and the tracking error is depicted in Fig. 4, which shows a rail-to-rail input and output range with lower than 2 mV tracking error. If 3.3V full swing is used to realize 256 grey levels for each color, this buffer amplifier has an accuracy within 0.16 LSB.

Driving capacity is simulated under various circumstances. Figure 5 shows the simulated output with a 20 kHz, 0-3.3 V triangular input signal, under a load capacitance of 600 pF. It is shown that the output follows the input signal well. Figure 6 shows the responses of 50 kHz, 20 mV step signal. It can be seen that the buffer is capable to sense small input difference. Simulations of 20mV step signals in regions both near the VDD and GND was taken. When only n-type or p-type input stage works, the buffer amplifier still works well. Step response of large signal transition is shown in Fig. 7 and Fig. 8, with a 50 kHz, 0-3.3 V square wave and 600 pF/30 pF load capacitance. They show that the proposed buffer amplifier is stable under both small and large loading capacitance.

Settling times, defined as the time for the output to settle down on the rising and falling edge with in 0.2% of full voltage swing, are depicted in Fig. 9, with respect to different load capacitances. The settling times with 600 pF load capacitance are 2.0 μs and 2.6 μs for the rising and falling edge. Even at a load of 1000 pF, the settling time is only about 2.8/3.6 μs . The inequality of settling times during rising and falling edges raises from the vertically asymmetry of the current summing circuit. However, it is known that a 1600*1200(UXGA) LCD display requires a horizontal scanning time of 9.877 μs [3]. The proposed amplifier is adequate for large display drivers.

III. COMPARISON

Performance comparison with existing buffer amplifiers for LCD column drivers is shown in Table I. The result shows that

TABLE I
COMPARISON WITH OTHER REPORTED BUFFER AMPLIFIERS FOR LCD COLUMN DRIVER.

	This work	Lu et al. [4]	Itakura et al. [8]	Weng et al. [7]
Technology	0.35 μm CMOS	0.35 μm CMOS	0.6 μm CMOS	0.35 μm CMOS
Vdd	3.3V	3.3 V	5 V	3.3 V
Input/output swing range	100% of Vdd	100% of Vdd	80 % of Vdd	97 % of Vdd
Quiescent current	2.0 μA	7 μA	8.2 μA	7.4 μA
Settling time	1.5 μs (rise) 2.1 μs (fall) ($C_L=600$ pF)	2.7 μs (rise) 2.9 μs (fall) ($C_L=600$ pF)	8.3 μs ($C_L=30$ pF)	8 μs ($C_L=600$ pF)

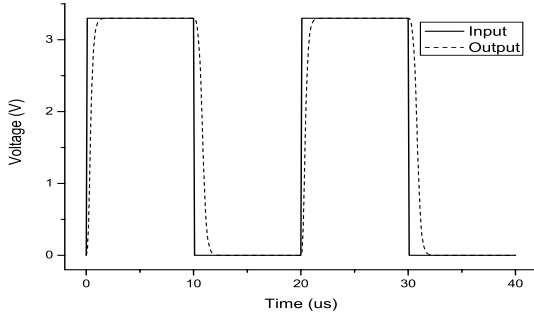


Fig. 7. Large scale step response, 600 pF load capacitance.

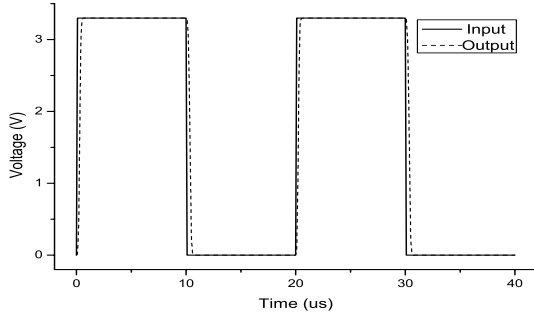


Fig. 8. Large scale step response, 30 pF load capacitance.

the proposed amplifier is superior in static power consumption and settling time. Compared with [4], the static power is reduced by 71 %.

IV. CONCLUSIONS

A low-power high-speed rail-to-rail buffer amplifier for LCD column driver is proposed. By utilizing a improved current summing circuit with embedded comparators, the buffer amplifier has fast and large driving capacity and drives little quiescent current, without paying for extra silicon area or complex architecture. Simulation with 0.35 μm CMOS technology shows that the circuit draws only 2.0 μA at static state, under a power supply of 3.3 V. The buffer amplifier has rail-to-rail input range with maximum tracking error of 0.16 LSB. In addition, it can drive a wide range of capacitive load, which indicates its potential in different size panels. Simulation results also show that it exhibits a settling time of 2.0 μs for rising and 3.1 μs for falling edge under voltage

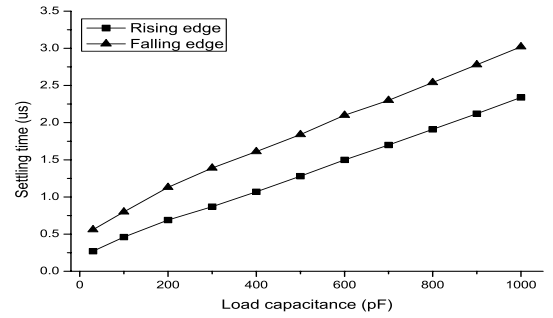


Fig. 9. Settling times with different load capacitances

swing of 3.3 V within $\pm 0.2\%$ with 600 pF load capacitance. Compared with existing buffer amplifiers for LCD applications, this work is superior in static power consumption, input range and settling time. The proposed buffer amplifier can be an appropriate candidate for LCD source drivers.

ACKNOWLEDGMENT

The chip design in this work is supported by VLSI Design and Education Center(VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc.

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