Crosstalk Analysis of Through Silicon Vias With Low Pitch-to-diameter ratio in 3D-IC

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Abstract- **An equivalent circuit model for low pitch-to-diameter ratio (P/D) through silicon via (TSV) in three-dimensional integrated circuit (3-D IC) is proposed in this paper. The shunt admittance of this model is calculated based on the method of moments which can accurately capture the proximity effect for both a TSV pair and TSV array. The metal-oxide-semiconductor (MOS) capacitance of TSV is also considered. With this model, the crosstalk of TSV array can be fully analyzed regardless of the pitch. The results by this model agree well with those by the electromagnetic simulations up to 40GHz.**

I. INTRODUCTION

Through silicon via (TSV) technology has proven to be the key point of three-dimensional integrated circuit (3-D IC), especially for high performance, more functionality and compact 3-D ICs. In TSV-based 3D-IC, there are large amounts of signal/ground and power/ground TSV pair and TSV array, to connect chips vertically with shortened electrical delay and provide extremely dense I/O connections. With the fabrication technique being enhanced, TSVs with high aspect ratio and low pitch-to-diameter ratio (P/D) will become the main stream of the high performance system with wide I/O bus on 3-D IC [1].

In order to evaluate the electrical behavior for TSV-based 3D-IC, it is desirable to have an equivalent circuit model for TSVs. Usually the model of two parallel wire and coaxial line is employed (e.g., [2-3]) for high pitch-to-diameter ratio of a TSV pair and TSV array, under the assumption that the circular interface between the insulator layer and the silicon substrate of TSVs has equal potential or is like a metal interface. For low pitch-to-diameter ratio of TSVs, however, this assumption would not be valid because of the strong electric-field interaction. Hence, Cheng et al [1] used conformal mapping method to obtain the equivalent capacitance and conductance of a TSV pair in this case. However, it is difficult to find the conformal mapping formula for TSV array.

In this paper, an equivalent circuit model for TSV structure with low P/D is proposed. The shunt admittance of TSV without depletion region [4] is calculated by the method of moments previously used for the single layer dielectric-coated wires [5]. We extend this method to calculate the admittance of double layers dielectric-coated wire in this paper, resulting that both the oxide and metal-oxide-semiconductor (MOS) capacitance of TSVs can be considered in the equivalent circuit model. For both a TSV pair and TSV array with low P/D, the non-uniform charge distributions on conductor peripheries due to the proximity effect are completely considered. Based on this model, the crosstalk among TSVs can be fully analyzed regardless of the pitch.

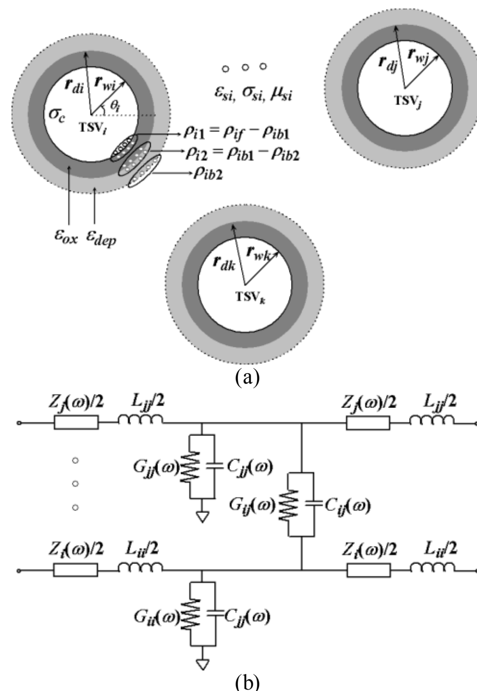

Figure 1. (a) The cross-section view of *n* TSVs with charge distributions at the three interfaces. (b) Equivalent circuit model for TSV structure (the mutual inductance is not shown for clarity).

II. EQUIVALENT CIRCUIT MODEL FOR TSVS WITH LOW P/D

For an array of *n* TSVs in Fig. 1(a), the equivalent circuit model is proposed and shown in Fig. 1(b). Unlike those of [1-3], the admittance of this model can be directly calculated and it is the sum of the oxide capacitance, MOS capacitance, silicon substrate capacitance and conductance. Since the geometry size of TSV structure is small enough compared with the wavelength at the frequency of interest, these frequency dependent *RLCG* parameters are computed under the quasi-static assumption.

A. Capacitance and Conductance

For each TSV in Fig. 1(a), there are three interfaces: conductor-oxide, oxide-depletion region and depletion region-

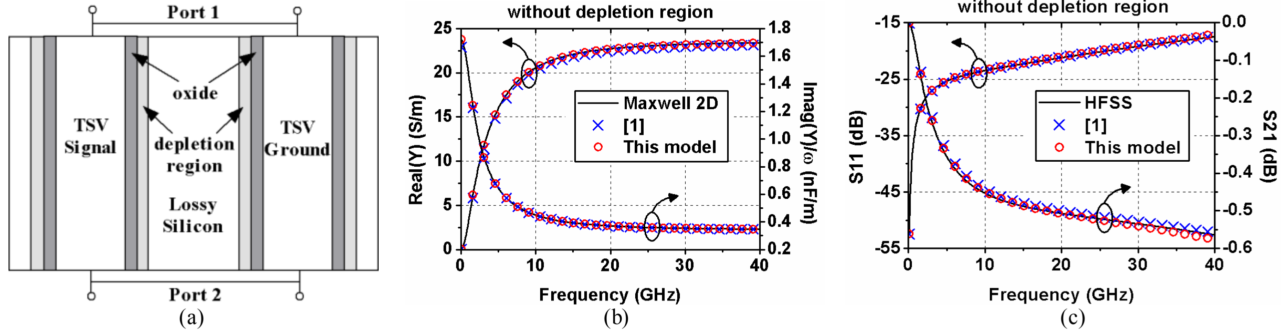

Figure 2. (a) Structure of a signal/ground TSV pair. Comparison of (b) the shunt admittance without depletion region by this model and Maxwell 2D, (c) the S parameters without depletion region by this model and HFSS. The results by conformal mapping method [1] are also added for comparison.

lossy silicon. The key point of handling this inhomogeneous structure is to replace the interface with the bound charge at these three interfaces.

As shown in Fig. 1(a), the charge distribution $\rho_{i1}(\theta_i)$ at the conductor-oxide interface contain the free charge $\rho_{if}(\theta_i)$ and oxide bound charge $-\rho_{ib1}(\theta_i)$, while the charge distribution $\rho_{i2}(\theta_i)$ at the oxide-depletion region interface contain the oxide and depletion region bound charge $\rho_{ib1}(\theta_i)$, $-\rho_{ib2}(\theta_i)$, respectively. These charge distribution can be expanded into a Fourier series [5] and must meet two boundary conditions: (a) potential at observation points of each conductor surface is equal, and (b) normal component of the displacement vector is continuous at the observation points on two dielectric interfaces. This will give the generalized capacitance matrix for n TSVs with the same form [5]:

$$\begin{bmatrix} q_{1f} \\ q_{2f} \\ \vdots \\ q_{nf} \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} & \cdots & C_{1n} \\ C_{21} & C_{22} & & \vdots \\ \vdots & & \ddots & \vdots \\ C_{n1} & \cdots & \cdots & C_{nn} \end{bmatrix} \begin{bmatrix} \phi_1 \\ \phi_2 \\ \vdots \\ \phi_n \end{bmatrix} \quad (1)$$

where q_{if}, ϕ_i are the per-unit-length free charge and potential on the conductor of the ith TSV respectively. C_{ij} is the capacitance coefficient established by the above two boundary conditions.

With the complex permittivity of the silicon

$$\varepsilon_{si}^{*} = \varepsilon_{si} - j\frac{\sigma_{si}}{\omega} \quad (2)$$

a complex capacitance matrix C^* can be directly calculated from (1). And from this complex capacitance matrix, we have

$$C = \mathrm{Re}(C^*) \text{ and } G = -\omega \cdot \mathrm{Im}(C^*) \quad (3)$$

where $\omega=2\pi f$ is the angular frequency of interest.

B. Inductance and Resistance

The per-unit-length inductance matrix L can be obtained from the duality of

$$L = \mu_0 \varepsilon_0 C_0^{-1} \quad (4)$$

where C_0 is the capacitance matrix with the oxide and silicon surrounding the TSVs removed.

The internal impedance of the TSV is calculated by the formula [6]:

$$Z = \frac{\sqrt{j\omega\mu\sigma_c}}{2\pi r_w} \frac{I_0(j\omega\mu\sigma_c)}{I_1(j\omega\mu\sigma_c)} \quad (5)$$

where σ_c is the conductivity of the TSV metal. I_0 and I_1 are, respectively, the modified Bessel functions of order zero and one, and r_w is the radius of the TSV.

III. Analysis of TSVs with Low P/D

A. A TSV Pair

A TSV pair with geometric parameters same as [1] are chosen to verify the accuracy of our model. As shown in Fig. 2(a), the TSV pair is 100 µm in height, while the diameter and pitch of each TSV are 30 µm and 40 µm, respectively. The conductivity of silicon is 10 S/m, where the relative permittivity of the silicon and oxide are 11.9 and 4, respectively. The maximum depletion width is 0.79 µm by the formula in [6].

To compare with the conformal mapping method [1] which does not consider the depletion region, the equivalent shunt admittance is obtained by this model and MAXWELL 2D [7], as shown in Fig. 2(b). Fig. 2(c) shows the corresponding S-parameters calculated and compared with HFSS [8]. As can be seen, all the results show good agreements.

To evaluate the effect of depletion region, Fig. 3(a) shows the comparison of the insertion loss (S21) of TSV pair with and without depletion region under different P/D at 10GHz. As can be seen, the difference between the S21 with and without depletion region will increase slightly from 0.01dB to 0.07dB as the P/D decreases from 3 to 1.2. One can also observe that the S21 is in the range of 0.3-0.46 dB, which means that the insertion loss is not very large when the P/D varies from 3 to 1.2.

If several chips are stacked and connected by the TSV pair, the total length of the TSV will affect the insertion loss S21, as illustrated in Fig. 3(b), which shows the tendency of S21 with the number of stacked chips (N_c) for P/D=1.33 at 10GHz. The microbumps are ignored in this paper for simplicity. For the case of without depletion region, the insertion loss increases from around 0.45 dB to 3.2 dB when the number of stacked chips increases. Meanwhile, the difference between the S21 with and without depletion region increases from 0.05 dB (N_c=1) to 0.3 dB (N_c=8).

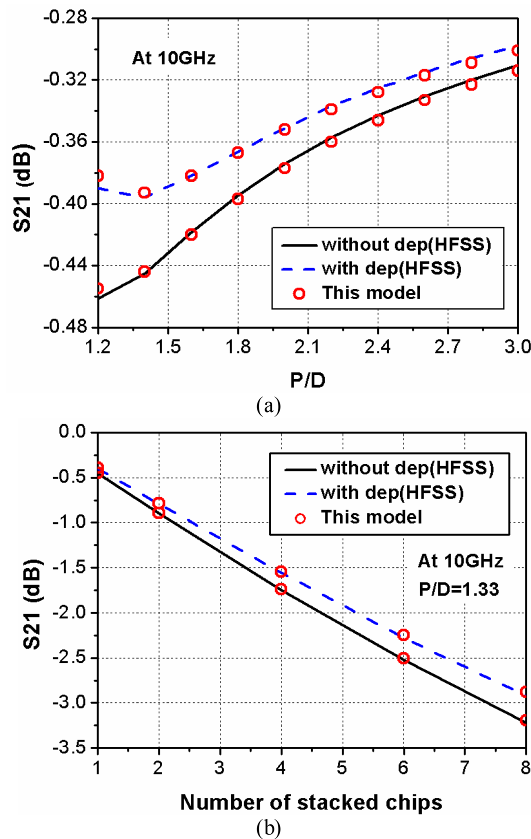

Figure 3. The S21 of the TSV pair with and without depletion region under (a) different P/D at 10GHz (b) different number of stacked chips with P/D=1.33 at 10GHz.

B. TSV array

As stated in section I, it is difficult to find a conformal mapping formula for TSV array with low P/D. Fig. 4(a) shows such a TSV array with 5 signal TSVs and 1 grounded TSV for reference. It is like that of [6], but the P/D of TSVs has been reduced from 10 in [6] to 1.33. The thickness of the oxide, depletion region and the diameter of each TSV are the same as that in the last example of section III A.

Though the significance of crosstalk noise depends on the products and applications, it becomes a concern when its level is in a range between -60 dB and -26 dB in the frequency domain or 0.1% and 5% of the supply voltage in time domain in general [9]. In frequency domain, the near-end crosstalk (NEXT) and far-end crosstalk (FEXT) between TSV_1 (aggressor) and TSV_i ($i \neq 1$, victim) are evaluated using this model and given in Fig. 4(b). The results by this model are in good agreement with that by HFSS. It can be observed that NEXT is higher than FEXT for all cases. And both NEXT and FEXT affect the nearest victim most. Meanwhile, higher frequency strengthens both the capacitive and magnetic coupling between aggressor and victim, which leads to the crosstalk increasing with the frequency. As can be seen from Fig. 4(b), the NEXT and FEXT between TSV_1 and TSV_2 both exceed -60 dB at 0.2 GHz and reach to -16.6 dB and -22.3 dB at 40 GHz respectively.

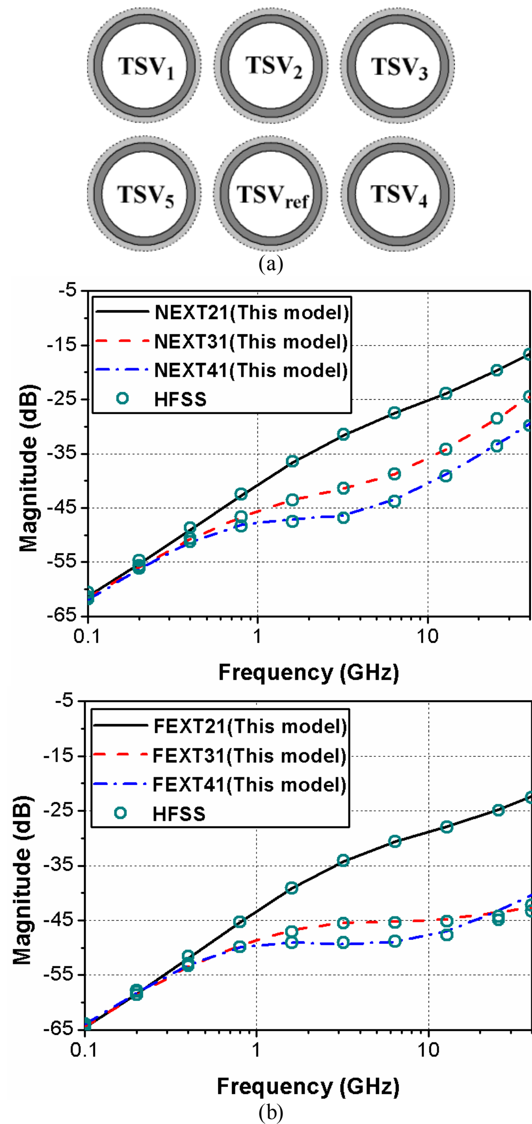

Figure 4. (a) TSV array with 5 signal TSVs and 1 grounded TSV for reference. (b) Magnitude of near-end crosstalk (NEXT) and far-end crosstalk (FEXT) between TSV_1 and TSV_i ($i \neq 1$) with P/D=1.33.

In order to evaluate the crosstalk between TSV_1 and TSV_2 (P/D=1.33) in time domain, a step signal of 1V is injected into TSV_1. All TSVs are terminated at both ends by a 50 Ω resistance. With the rise time of the signal decreasing, the peak value of both the NEXT and FEXT on TSV_2 increase and reach beyond 1% of the supply voltage when the rise time is 30 ps, as shown in Fig. 5. This is due to that the higher frequency component contained in the signal of lower rise time will cause higher noise level on adjacent TSV, as can be seen in Fig. 4(b). It should be noticed that the noise margin of a gate depends on both the peak amplitude of noise and its duration. For example, digital circuits can often tolerate (and indeed filter out) spike-like crosstalk noise with a large peak amplitude and very small noise width, as indicated in [10]. Thus, comprehensive evaluation are needed for the crosstalk in TSV interconnect.

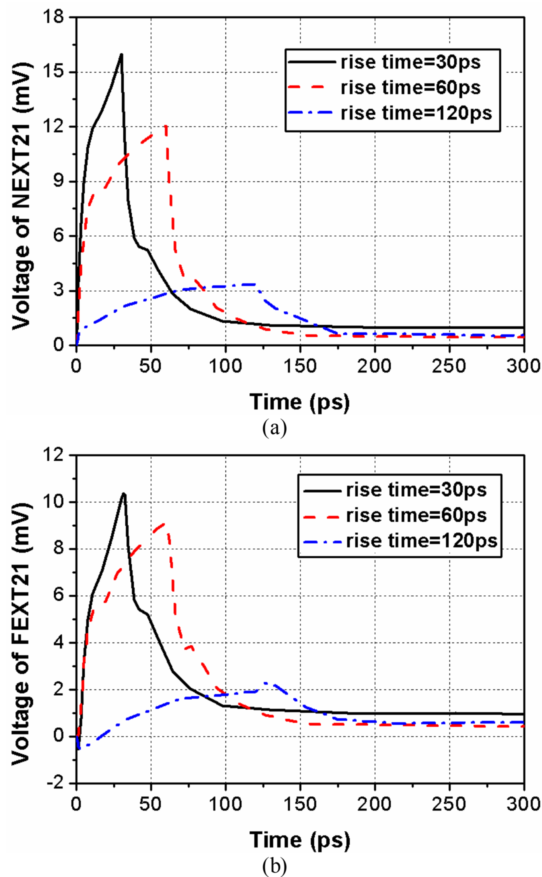

Fig. 5 Time domain voltage of (a) NEXT and (b) FEXT between TSV_1 and TSV_2 (P/D=1.33) for different rise time of a step signal.

IV. CONCLUSION

The equivalent circuit model for low P/D TSV structure has been proposed. For both a TSV pair and TSV array with low P/D, the proximity effect on the shunt admittance of TSVs with depletion region is rigorously considered by the method of moments. The crosstalk behavior of TSV array with low P/D has also been analyzed in both frequency domain and time domain. Results by this model show good agreements with those of electromagnetic simulations.

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