Improvement of ESD Robustness in Gallium Nitride-based Flip-Chip HEMT by Introducing Metal-Insulator-Metal Capacitor

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***Abstract*—We report on improvement of ESD characteristics of AlGaN/GaN high-electron mobility transistor (HEMT) using metal-insulator-metal (MIM) structure aluminium nitride (AlN) flip-chip (FC) submount. Compared with FC-free HEMT, measured results of the FC HEMT show the improvements of 25 and 150% under drain-to-source and gate-to- source electrostatic discharge (ESD) stress respectively, which is attributed to an extra path formed in the MIM structure AlN FC submount to flow the ESD current and to support the charge by the additional capacitances.**

Keywords*—*HEMT; Flip-Chip; ESD; AlGaN/GaN; AlN; Capacitor

I. INTRODUCTION

AlGaN/GaN high electron mobility transistor (HEMT) has shown an excellent promise for high frequency and high power applications. However, a crucial technology challenge for its further success is the reliability under either a thermally activated effect or a high-voltage stress [1]-[4]. Thus, there is still a need to find out new solutions for solving these reported problems. An efficient thermal management of AlGaN/GaN HEMT has been demonstrated by using a higher thermal conductivity material as the substrate [5] or a laser lift-off approach for replacing the original substrate [6]. In addition, for realizing the cost-effective and high-performance GaN-based power devices, the optimized flip-chip (FC) designs with an improved thermal performance are proposed [7],[8]. By providing an efficient heat sink via the bumps, the adversely thermal effect in the device can be significantly reduced. Furthermore, a number of electrostatic discharge (ESD) protection circuits based on FC configuration are also presented in light-emitting diode (LED) [9]-[12] technologies.

In this paper, an AlGaN/GaN HEMT integrated with a metal-insulator-metal (MIM) structure AlN FC submount using FC bumps is proposed to improve the ESD characteristics. In addition, we also investigated the improvements of ESD characteristics of the FC HEMT through the ESD robustness experiments. When the FC HEMT is under a high voltage ESD stress at a very high frequency region, an external ESD stress bypass path will be formed in the proposed MIM structure AlN FC submount according to the impedance formula $Z_c = 1/j\omega C$.

II. EXPERIMENTAL PROCEDURE

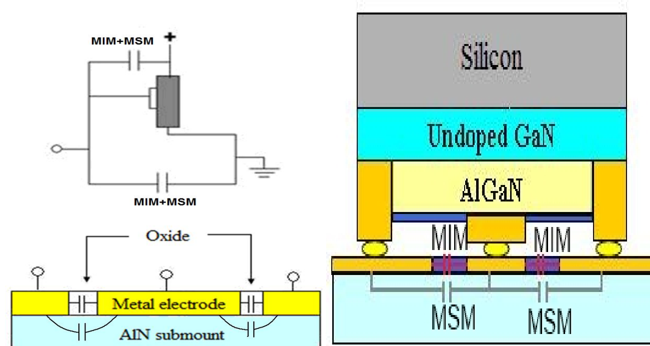

Fig. 1. Schematic diagrams of the proposed AlGaN/GaN FC HEMT using the MIM structure AlN FC submount.

Fig. 1. shows the schematic diagrams of the proposed AlGaN/GaN FC HEMT in this study. An $Al_{0.26}Ga_{0.74}N$ (25nm) / GaN (2μm) heterostructure grown by MOCVD on Si substrate was used. Ni/Au was used as the gate Schottky

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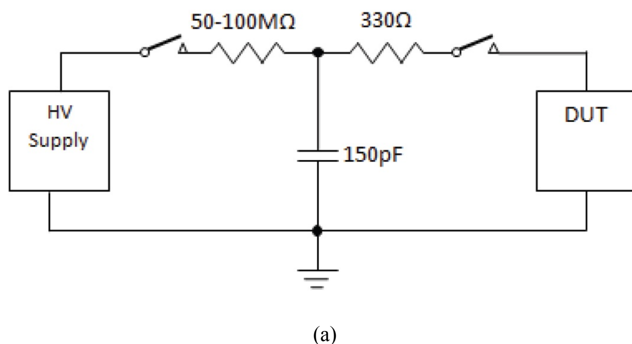
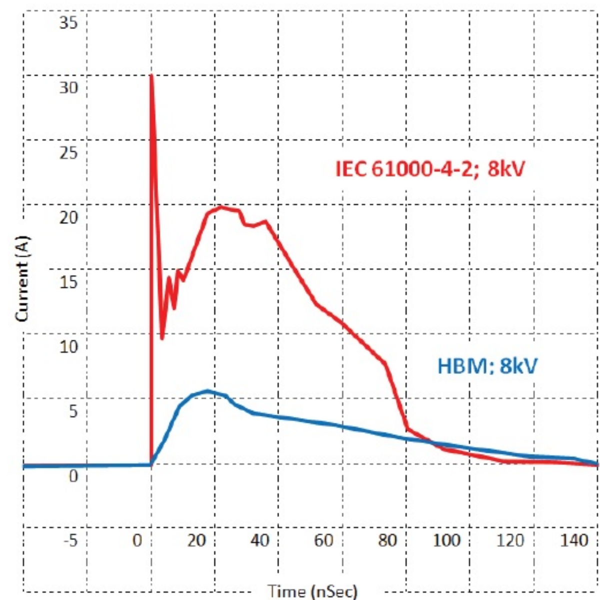
contact, and the source and drain ohmic contacts were made of Ti/Al/Ni/Au. On top of the AlGaN, a 120 nm thick SiN_x passivation layer was grown. The gate widths of either 1 or 2 mm were designed to investigate whether the reported improvements of ESD characteristics are significant device to device. Many ESD standards such as Human Body Model (HBM), Machine Model (MM), Charged Device Model (CDM) and IEC 61000-4-2 have been developed to test the performance and robustness of electronic devices. In addition, the gate-source and gate-drain separation, and gate length were 2, 3, and 1.2 μm, respectively. Moreover, for constructing the MIM structures, a 1000 Å-thick SiO_2 insulator layer was deposited on the AlN submount with a 1000 ^{o}C post-annealing of 10 min, followed by photo lithography to pattern the corresponding electrodes. After a RIE process, 1000 Å-thick Ti/Au electrodes were obtained by using an e-gun evaporator, followed by an excess-metal liftoff process and a 400 ^{o}C RTA process of 30 s. Furthermore, for the FC connection, a wire bonder was used to deposit the gold bumps on the gate, drain, and source electrodes respectively, followed by using the thermosonic FC bonding processes [13] with the optimized process parameters of AlN FC submount heating of 150 ^{o}C, force of 550 g, power of 11.9 W, and press time of 5 ms.

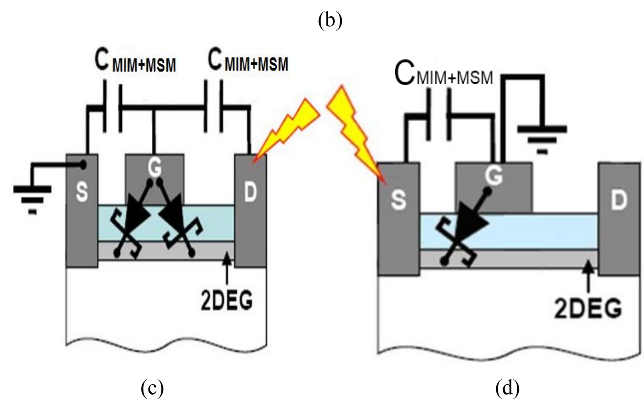
In the ESD robustness experiments, we used an ESD simulator (KeyTek MiniZap MZ-15/EC) to add the simulator signal to the device under test (DUT) by air discharge. The ESD gun is brought close to the pin until there is a discharge to the pin, as shown in Fig. 2. (a). Even at the same applied voltage (ex.8kV), the peak current of the actual ESD signal (MIL-STD-883 human body model, HBM) is less than five times of the simulator output (IEC 61000-4-2) , as shown in Fig. 2. (b). In order to test the ESD characteristics of the proposed FC HEMT in two different configurations referring to the reported articles [4],[14] : (a) positive voltage pulse which was considered to be ESD stress applied to the drain with source grounded and gate floating for evaluating the increased ESD robustness of the whole device structure; (b) positive voltage pulse which was considered to be ESD stress applied to the source with gate grounded and drain floating for evaluating the increased ESD robustness of the Schottky diode, as shown in Fig. 2. (c) and (d) respectively. Meanwhile, the fail criterions are used as the I_{ds} = 0 A and the leakage current greater than the value of 10^{-5} A, called the absolute-leakage-current method [15], respectively.



(a)



(b)



(c) (d)

Fig. 2. (a) Equivalent circuit of the ESD simulator meeting the requirement of IEC 61000-4-2 (HBM) with rise-time of 0.7 ~ 1 ns. (b)At the 8kV ESD voltage, the peak current of MIL-STD-883 (HBM) and IEC 61000-4-2 are 5.33A and 30A, respectively. And the schematic diagrams of applying (c) drain-to-source ESD stress to 2DEG channel and (d) gate-to- source ESD stress to Schottky diode.

III. RESULTS AND DISCUSSION

In the DC characteristics measurements, it is observed that the FC HEMT shows the improvements of 44, 30, and 85% in I_{ds}-V_{ds}, I_{ds}-V_{gs}, and g_m-V_{gs} characteristics respectively than that of the FC-free HEMT, as shown in Fig. 3. . These results reveal that the proposed FC HEMT has the improved thermal performances as Das et al. reported [17]. In addition, due to the similar turn-on voltage (I_G = 1 mA/mm) of -1.15 V appearing on both the FC and FC-free HEMTs, the flip-chip-integration approach used in this study has less influence on the inherent property of the HEMT.

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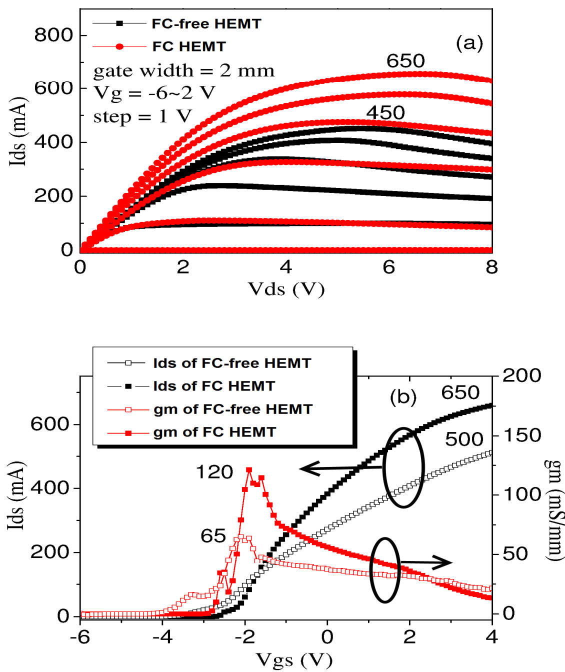
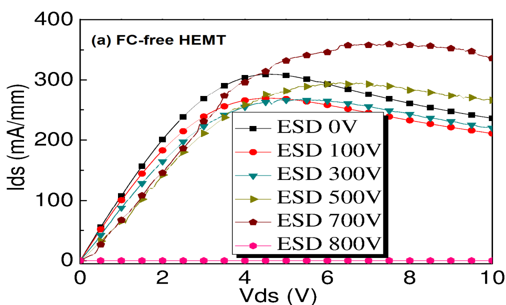


Fig. 3. Measured (a) I_{ds}-V_{ds} characteristics and (b) I_{ds}-V_{gs} and g_m-V_{gs} characteristics of the FC-free and FC HEMT (gate width = 2 mm).

In the ESD robustness experiments, we applied the ESD stresses to the two-dimensional electron gas (2DEG) channel and gate-to-source Schottky diode respectively for evaluating the improved ESD robustness of the FC HEMT as compared with the FC-free HEMT. In Fig. 4.(a), we observe that the 2DEG channel of the FC-free HEMT fails when the applied ESD stress reaches the value of 800 V, whereas that of the FC HEMT fails when the applied ESD stress reaches the value of 1000 V. We believe that the 25% improvement of ESD robustness of the 2DEG channel of the FC HEMT mainly stems from the extra ESD stress bypassing path formed in the MIM structure AlN FC submount to flow the ESD current and to support the charge by the increased capacitance (estimated ~3 pF) as compared with the intrinsic gate-to-source or gate-to-drain capacitances (under 1 pF mostly) of the FC-free HEMT. We also found that the FC HEMT has the less variance in I_{ds}, as shown in Fig. 4.(b), than that of the FC-free HEMT. It suggests that the robust DC performances and ESD characteristics can be obtained simultaneously in the proposed FC HEMT.



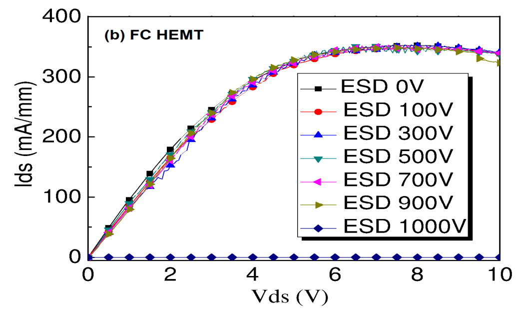


Fig. 4. Measured I_{ds}-V_{ds} characteristics as a function of drain-to-source ESD stress magnitude for the (a) FC-free and (b) FC HEMT (gate width = 1 mm).

As shown in Fig. 5.(a), the resulted leakage current of FC-free HEMT meets the failure criterion as an applied ESD stress of 100 V, whereas that of FC HEMT meets the failure criterion as an applied ESD stress of 250 V, as shown in Fig. 5.(b). We reasons that the 150% improvement of ESD robustness of the gate-to-source Schottky diode of the FC HEMT is also due to the extra ESD stress bypassing path formed in the MIM structure AlN FC submount. Based on these results presented in Figs. 4. and 5., the proposed FC HEMT has effectively improved the ESD robustness.

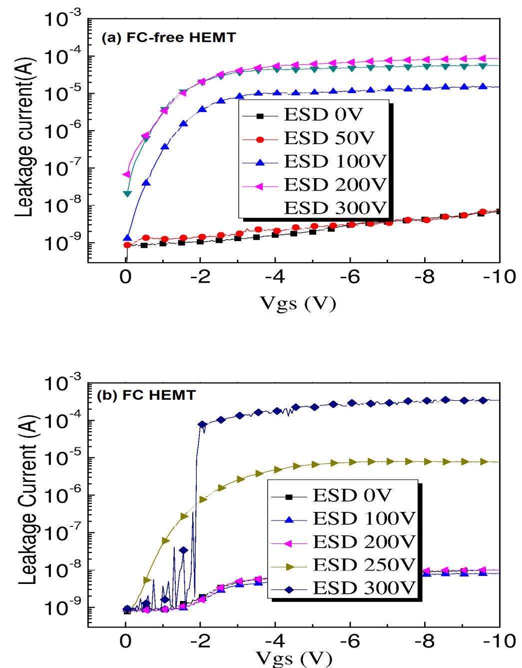


Fig. 5. (Color online) Measured I_g-V_{gs} characteristics as a function of gate-to-source ESD stress magnitude for the (a) FC-free and (b) FC HEMT (gate width = 2 mm).

IV. CONCLUSIONS

An ESD protection device formed by MIM capacitors on the AlN submount is demonstrated to improve the ESD characteristics of the AlGaN/GaN HEMT. In addition, the

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improved thermal performances, including I_{ds} and g_m , have also been verified in the proposed FC HEMT by using the high thermal conductivity AlN submount. Using the proposed MIM capacitors and AlN submount, the ESD robustness and the adverse thermal influence of the FC-free HEMT can be improved at the same time. However, to our knowledge, the ESD stress handling capability of the MIM capacitors is directly proportional to the value of capacitance [13]. A tradeoff between ESD stress handling capability and parasitic capacitance effect caused by the introduced capacitors is suggested to take a further consideration. Furthermore, the impedance matching design between HEMT and AlN submount for obtaining the optimized output power (P_{out}) and the detailed analysis of the device parameters of the FC and FC-free HEMT for showing good agreement with measurement results need further investigation.

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