An Ultra-wideband CMOS Low-noise Amplifier with On-chip ESD Protection

Yu-Tsung Lo and Jean-Fu Kiang
Department of Electrical Engineering and Graduate Institute of Communication Engineering, National Taiwan University
E-mail: jfkiang@cc.ee.ntu.edu.tw.

Introduction

Ultra-wideband (UWB) radio technology can achieve high data rate with low radiation power. Many UWB LNAs have been proposed recently, but most of them are lack of ESD protection. In this work, an UWB LNA covering the bandwidth of 3.1-10.6 GHz is proposed. Sufficient gain is needed to lower the input-referred noise from the subsequent stages of the receiver. The noise figure of the LNA must be minimized to enhance its sensitivity and data rate. The proposed LNA is fully protected at RF ports and dc pads using the inductors and gate-couple NMOS [1], respectively.

1 ESD Protection Concepts

For ESD performance in RF applications, different protection schemes have to be used in RF ports and dc pads, seperately. Conventional ESD protection ciruits like diodes and gate-grounded NMOS (ggNMOS) can not be adopted to RF protection due to their parasitic capacitance [2]. On the other hand, inductors can be used as ESD protection circuit since the frequency characteristics of inductors in conventional RF circuits also meet the design requirement for ESD protection, namely, high impedance under normal operation of the protected circuit and low impedance to shunt the ESD stress. The duration of typical ESD impulses in the transmission line testing model is about 100 ns, with rise time of about 10 ns [1], thus the maximum voltage change rate is 1/10 ns = 100 MHz, much lower than 5 GHz. The inductor-based protection circuit can thus exhibit high impedance of $j2\pi(5G)L$ at normal states and low impedance $j2\pi(100M)L$ during ESD events. To analyze the ESD performance in dc pads, the spice model for typical MOSFET is lack of avalanche breakdown mechanism, hence must be modified to fit our purpose.

2 Architecture

Fig. 1 shows the proposed UWB LNA, which has the first stage made of common-gate topology and the second stage made of cascode topology. Wideband input impedance matching can be achieved by choosing the common-gate topology. Neglecting the input coupling capacitance and the loading effect at the first stage, the input impedance can be expressed as [3]

$$Z_{in} = \frac{sL_{s1}}{1 + (g_{m1} + sC_{gs1})sL_{s1}}$$

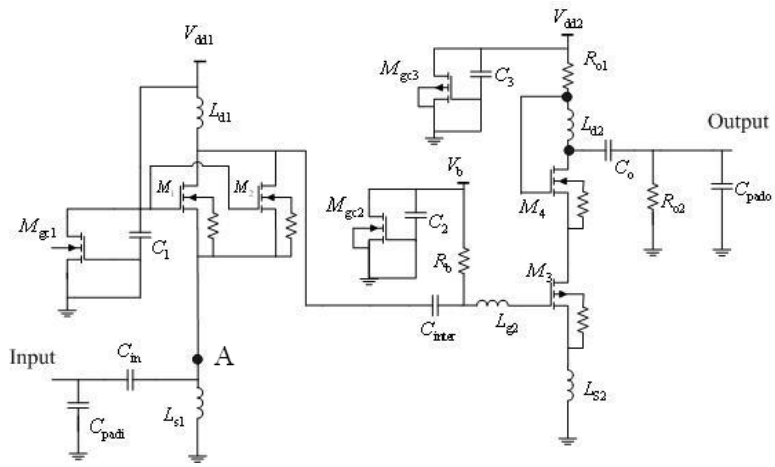

Figure 1: Architecture of the proposed LNA.

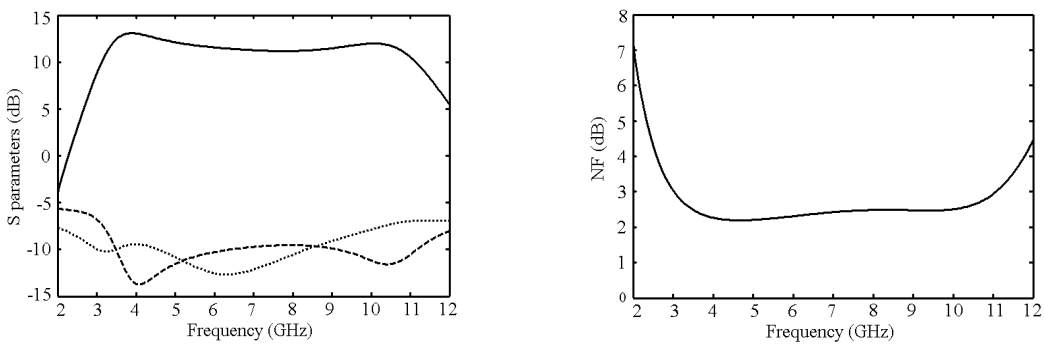

Figure 2: S-parameters and noise figure.

where g_{m1} and C_{gs1} are the transconductance and the gate-source parasitic capacitance, respetively, of transistor M_1. Using the common-gate topology at the input stage not only provides a wideband input matching, but also provides ESD protection capability at the RF port, because the inductor at the source of M_1 is connected to a shunting current path. Thus, no additional ESD protection inductor is needed.

3 Simulation Results

As shown in Fig.2, the power gain of the proposed LNA is between 10.6 dB to 13 dB in 3.1-10.6GHz, the return losses S_{11} and S_{22} are below -8 dB and -7.2 dB, respectively. The minimum and the maxmum noise figures are 2.2 and 2.8, respectively. The 1-dB compression point is -10.6 dBm, and the third order intermodulation IIP3 is -4.38 dBm, which are simulated at 6 GHz.

To test the ESD performance, an ESD impulse based on human body model [4] are fed into the RF port. The ESD impulse at node A sees a dc blocking capacitance C_{indc}=4 pF and an equivalent pad parasitic capacotance C_{padi}=30 fF. Most induced current will go through C_{indc} due to its much larger capacitance. The relation

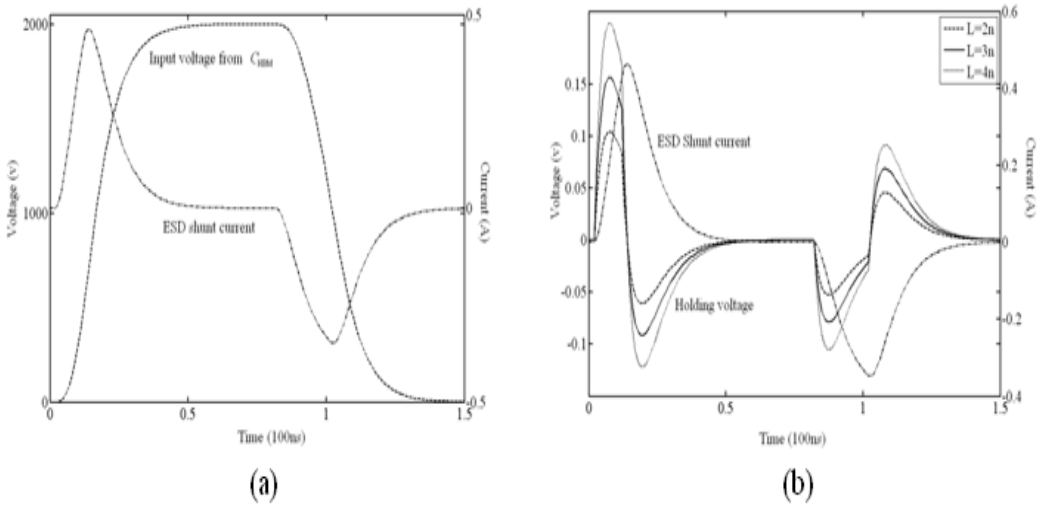

Figure 3: Induced current through L_{s1} and voltage at node A.

Table 1: Performance of the Proposed LNA.

Parameter	[3]	[5]	[6]	This work
CMOS Technology	0.18 μm	0.18 μm	0.18 μm	0.18 μm
Supply voltage (V)	1.8	1.2	1.5	1.5
BW (GHz)	0.4-10	2-11.5	2.9-11	3.1-10.6
gain (dB)	11.2-12.4	10-14.8	16***	10.6-13
Noise figure (dB)	4.4-6.5	3.1-4.1	3.8-4.0	2.2-2.8
S_{11}/S_{22} (dB)	$< -10/< -10$	$< -10/--$	$< -10/--$	$< -8/< -7.2$
$P_{1\text{dB}}$ (dBm)	$--$	-8.5	$--$	-10.6
IIP_3 (dBm)	-6	$+3$	$--$	-4.38
Circuit topology*	CG+C+B	C+SR	CG+CS+B	CG+C
Power (mW)	12*	13.4	9.5*	12
Chip area (mm^2)	0.42	0.33	0.984	0.68

$*$ C: cascode, B: buffer, SR: shunt resistive feedback.

between the input ESD impulse and the induced current through L_{s1} is shown on Fig.3(a).

Fig. 3(b) shows the current through L_{s1} and the voltage at node A, the latter has a very low value of less than 2 mV under a 2 kV HBM ESD impulse. Hence, the protected circuit is less likely to be damaged by an ESD. The damage may only occurs at the inductor by the large current induced by an ESD impulse. Thus, the inductor L_{s1} can shunt an ESD induced current and hold the voltage at node B under a very low level. Note that Fig. 3 reveals that the ESD protection performance is highly related to the value of inductors. The lower value leads to better ESD protection performance, but the differece of inductance is not critical enough to be traded off with its RF performance. Hence, when using CG topology with inductor at the first stage, the RF performance should be put in a higher priority, the effect of inductance value on ESD performance is apparent but not critical under HBM.

4 Conclusion

An UWB LNA with ESD protection mechanism is proposed. The ESD protection is applied on RF ports and dc pads. Simulation shows that an inductor can be used for ESD protection in an RFIC because its impedance level changes dramatically under an RF signal and an ESD impulse. The comparison with other state-of-the-art UWB LNAs is listed in Table .

References

[1] D. Linten et al, "A 5-GHz fully integrated ESD-protected low-noise amplifier in 90-nm RF CMOS," *IEEE Trans. JSSC*, vol.40, no.7, pp. 1434-1442, July 2005.

[2] A. Amerasekera and C. Duvvury, *ESD in Silicon Integrated Circuits*, Wiley, 2002.

[3] K. H. Chen, J. H. Lu, B. J. Chen, and S. I. Liu, "An ultra-wideband 0.4-10 GHz LNA in 0.18um CMOS," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 54, pp. 217-221, Mar. 2007.

[4] S .H. Voldman, *ESD Physics and Devices*, Wiley, 2004.

[5] H. K. Chen, D. C. Chang, Y. Z. Juang, and S. Sh. Lu, "A Compact wideband CMOS low-noise amplifier using shunt resistive-feedback and series inductive-peaking techniques," *IEEE Microwave Wireless Comp. Lett.*, vol.17, no.8, pp.616-618, Aug. 2007.

[6] Y. Shim, C. W. Kim, J. Lee, and S. G. Lee, "Design of full band UWB common-gate LNA," *IEEE Microwave Wireless Comp. Lett.*, vol.17, no.10, pp.721-723, Oct. 2007.