Injection-Locked-Based BPSK Demodulator in RFID Tag

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Introduction

PSK modulation is not usually used in the downlink (reader to tag) of typical RFID systems mainly because PSK demodulation takes a more complex detection scheme than ASK [1]. On the other hand, the PSK modulation becomes a good candidate in the uplink (tag to reader) because of its higher data rate and higher resilience against noise.

A power-efficient tag with BPSK modulator has been proposed [2]. For the reader, although power is a less stringent constraint compared to tags, a low power system is still preferred, especially implemented in wireless technology.

In this paper, a power-efficient BPSK demodulator is proposed in which non-coherent detection and injection-locked BPSK-to-ASK transform are adopted. No mixer, PLL or ADC is required, thus the circuit complexity is significantly reduced as compared to coherent detection scheme.

Architecture

The proposed BPSK demodulator includes an injection-locked BPSK-to-ASK converter and an ASK demodulator as shown in Fig.1. The injection-locked BPSK-to-ASK converter is composed of two voltage-controlled oscillators and an MOSFET combiner. The ASK demodulator contains an envelope detector, a comparator, and a limiter.

Injection-locked BPSK-to-ASK converter. Fig.2 shows the LC-based VCOs of the system. The free-running frequencies of VCO1 and VCO2 are designed at 1.27 GHz and 1.18 GHz, respectively, by applying different levels of $V_{\rm ctrl}$. The RF input signal at 2.45 GHz is coupled to the gate of $M_{\rm s}$. This injection signal locks the output frequencies of these two VCOs at nodes A and B, respectively, to half of the input frequency. Thus, the oscillation frequency of VCO1 changes from 1.27 GHz to 1.225 GHz, and that of VCO2 changes from 1.18 GHz to 1.225 GHz.

The VCOs' output can be represented as [3]

$$A(t) = C\exp\left\{j\left(2\pi f_{\rm lock}t + \theta_1/2 + \pi/4\right)\right\}$$
$$B(t) = C\exp\left\{j\left(2\pi f_{\rm lock}t + \theta_2/2 + \pi/4\right)\right\}$$

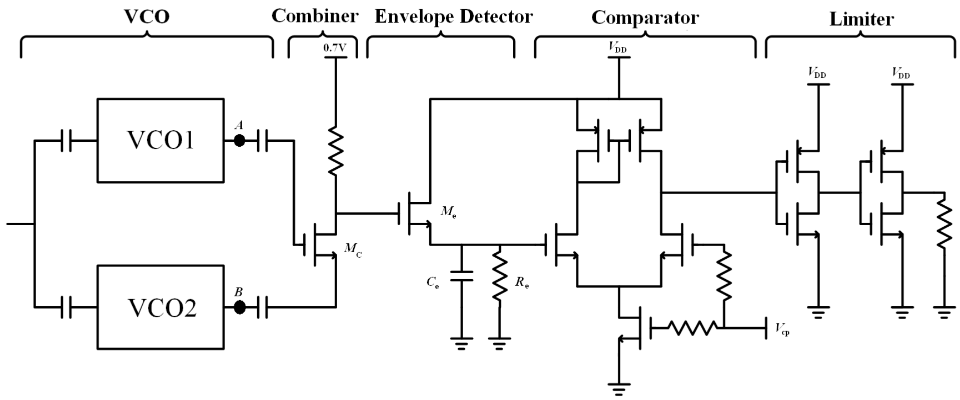

Figure 1: Architecture of the proposed BPSK demodulator.

If the phase of the input signal changes by 180° due to the BPSK modulation, the two outputs, $A(t)$ and $B(t)$, become

$$A(t) = C\exp\{j\,(2\pi f_{\text{lock}}t + \theta_1/2 + \pi/4 + \pi/2)\}$$
$$B(t) = C\exp\{j\,(2\pi f_{\text{lock}}t + \theta_2/2 + \pi/4 - \pi/2)\}$$

Thus, the 180° phase shift at the input signal causes the VCO outputs to change from in phase to out of phase, and the next phase change at the input will cause the two outputs to become in phase.

MOS combiner. A power combiner can be used to combine the signal at VCOs' output [4]. When $A(t)$ and $B(t)$ are in phase, the power combiner will generate a larger output amplitude than the case when $A(t)$ and $B(t)$ are out of phase. Thus, the BPSK input is converted to an ASK through injection-locked VCOs and a power combiner. While at the frequency of 2.45 GHz, on-chip realization of power combiner requires large silicon area. A new combiner specific to this system is proposed. A single MOS combiner is used to combine two VCOs' output to generate an ASK signal by connecting nodes A and B to the gate and drain of the MOS M_{C} as shown in Fig.1. When A and B are in phase, the MOS combiner M_{C} is turned off and its output voltage turns high. When A and B are out of phase, M_{C} is turned on and its output voltage turns low. Hence an ASK signal is generated without using a conventional power combiner.

ASK Demodulator

After the input BPSK signal is converted to an ASK signal, the next step will be to demodulate the ASK signal. An envelope detector composed of M_{e}, C_{e}, and R_{e} as shown in Fig.1 is an alternative to achieve this goal. A comparator following the envelope detector pulls the ASK signal to near rail-to-rail level. The decision boundary is about 0.6 V, given the voltage source V_{cp}. To enhance signal quality, a limiter composed of two inverters in cascade is used. Finally, the input BPSK signal is demodulated and a fine rail-to-rail digital signal is achieved.

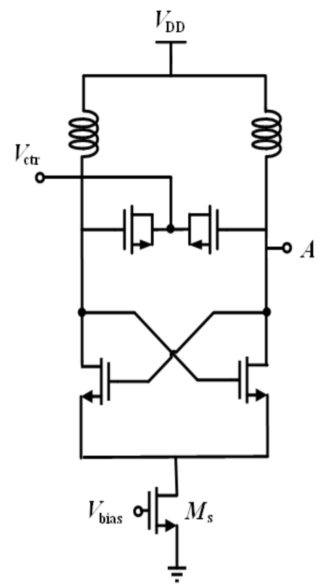

Figure 2: VCO used in the proposed system.

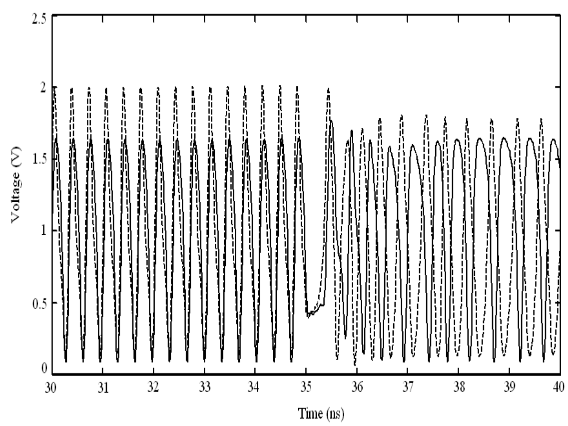

Figure 3: Output voltage of VCOs, $---$: $A(t)$, —: $B(t)$.

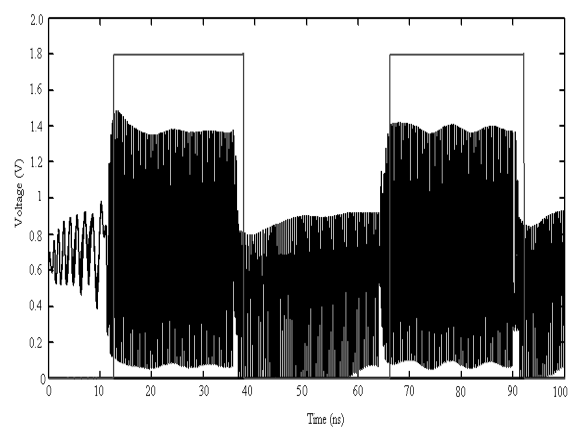

Figure 4: Output of MOS combiner and demodulated bit sequence.

Results and Conclusion

In the simulation, the RF input signal of 2.45 GHz is generated to carry a bit sequence 101010$\cdots$ with bit duration of 60 ns. During the phase change of the input BPSK signal, VCOs' output $A(t)$ and $B(t)$ change from in-phase to out-of-phase or from out-of-phase to in-phase as shown in Fig.3. The entire modulated input sequence causes the the phase of $A(t)$ and $B(t)$ to change back and forth. The MOS combiner combines $A(t)$ and $B(t)$ to generate an ASK signal with high level when $A(t)$ and $B(t)$ are in phase and low level when $A(t)$ and $B(t)$ are out of phase. The ASK signal is shown in Fig.4 together with the final digital output which is generated by the ASK demodulator. Thus, the BPSK signal is successfully demodulated to retrieve the original input bit sequence with the same bit duration and duty cycle.

The system is designed using TSMC 0.18μm RF/mixed signal technology. The supply voltage is $V_{\text{DD}} = 1.8$ V and the total power consumption is 9 mW, most of which is dissipated by the VCOs.

A noncoherent BPSK demodulator is designed. Compared to coherent detection which includes mixer, PLL, ADC in order to demodulate the original input sequence, the proposed architecture saves a lot of die area and hence cost. Since a BPSK-to-ASK converter is used, the digital signal can be retrieved without ADC. The small power consumption of 9 mW makes this design a good candidate for RFID tag system. Besides, the demodulator can provide a data rate up to 20 Mbps, which is beyond the requirement of all existing RFID protocals [5].

References

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