Realization of a SDR DBF for Micro-Satellite SAR on FPGA

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1. Introduction

On bi-static or multi-static space-borne radar the appropriate digital beam-former (DBF) algorithms can obtain multi-angular synthetic aperture radar (SAR) data and enhance signal-to-noise ratio. Some applications ask for short revisit time that need to ensure seamless coverage to obtain a wide swath SAR image data with a single satellite using digital beam-forming on receive scheme [1]. The transmitter and receiver antennas of the bi-static SAR for the micro-satellite can be mounted on a single carrier or placed on separate platforms [2]. Due to the reasons that the cross-track errors [3] of the distributed micro-satellite constellation and satellite fading channel errors will result in the phase difference among the received signals of each array antenna element, the proposed software defined radio (SDR) DBF is designed with the configuration of two antennas on a same micro-satellite. For the purpose of simplifying the phase compensation among the received signals from the array antenna elements and reducing the downlink transmission load, the proposed SDR DBF is to be realized on the board processor of micro-satellite. For micro-satellite SAR systems [4], power consumption is an important issue. The reconfigurable feature of the SDR architecture gives rise to reusability of hardware, scalability, and power efficiency [5]. Reusability of hardware supporting multiple modes of DBF strives for compactness and efficient power consumption. In this paper, according to the SDR architecture, a DBF system comprising multiple-beams, direction of arrival (DOA) estimation and null steering beam modes is realized using an field programmable gate array (FPGA) for the micro-satellite SAR system. In multiple-beam mode, the beam steering function is performed with high resolution. In DOA mode, the direction of the undesired interference signal is estimated using SAR receiver processing. In null steering beam mode, the receiver end on SAR can resist the interference to improve its anti-jamming capability. The mode could be chosen with software upgrading to achieve the hardware reconfiguration of the processing modules according to the variety of operation requirements.

2. Structure of SDR DBF

Fig. 1 shows the block diagram of SDR DBF. The reconfiguration controller is utilized for controlling the whole reconfiguration process of the SDR DBF by sending mode request command and reconfiguration command into interface processing unit. The memory of the interface processing unit resides application software code modules, which include 4-FFT code module MBF(θ_S), amplitude comparison DOA code module DOA(θ_L, θ_U) and null-steering beam-forming code module NSBF(θ_S, θ_n). The interface processing unit interfaces the SDR DBF with the reconfiguration controller, coordinates various data and controls information coming into and going out of the SDR DBF. The code modules, which are the parameterized program instructions, perform the FPGA reconfiguring and change the function of the SDR DBF. According to the SAR requirements, the reconfigurable controller sends mode request command to download a code module from the memory to interface processing unit, which translates code module as bit streams to set up the processing modules. Since the hardware reconfiguration has to be processed with

minimal delay and overheads, a SDR design requires partitioning the hardware circuits of the FPGA into small components. To reduce the reconfiguration time, the FPGA hardware of the SDR platform must be of modularized design. Different modes can share the common module operated with different parameters during mode switching. The use of FPGA is well aligned to the parallel nature of the applications. The FPGA is partitioned into three processing modules including multiple-beam, amplitude comparison DOA and null-steering modules as shown in Fig. 1. Each processing module attaches sufficient memory to store the bit streams, which are translated from the code module in the interface processing unit. Modular design of the functionality software code corresponding to each processing module of the DBF in FPGA for different modes will satisfy the reconfigurable requirements of the SDR platform when an update command arrives. The flow chart of the reconfiguration control algorithm is shown in Fig. 2.

3. Implementation of Multi-mode DBF on FPGA Processor

The example array antenna parameters for the micro-satellite SAR DBF system are given in [2]. The SAR uses an antenna array with N = 4 elements to receive echo. The cross-range transmit sampling distance of the SAR is $\Delta y_r = 0.5Nl_{rs}$ where l_{rs} is effective aperture of receiver antenna. The micro-satellite along track velocity v is assumed to be 7000 m/s [6]. The required processing time of SDR DBF should be less than the cross-range sampling time (PRI) $\Delta y_r / v$ = 40.36μsec for the four-element SAR antenna array. For a linear uniform array of N isotropic elements with the inter-element spacing d, the beam pattern is expressed as follows:

$$BF(\theta_s, m) = \sum_{n=0}^{N-1} x_n(m) e^{-jn\beta d \sin(\theta_s)} = \sum_{n=0}^{N-1} x_n(m) e^{\frac{-j2\pi ns}{N}}, \forall s = 0,1,\ldots,N-1 \tag{1}$$

where θ_s is the angle from the array broadside to the direction of far-field source; $\beta = 2\pi / \lambda$ is the phase propagation constant; λ is the wavelength of the carrier. $x_n(m)$, n = 0, 1,…, N– 1, which are the baseband output of n_{th} antenna element at m_{th} time instant, and input to N-FFT in parallel, generating N beams pointed at N different direction $\theta_s = \arcsin(s/N(d/\lambda))$, s = 0, 1,…, N– 1. The 14-bit fixed-point data format is employed to implement the 4-FFT on the FPGA processor. To speed up the processing time of the 4-FFT processing module, two-stage pipeline processing and two butterfly units in parallel per stage were used, allowing a 4-FFT computation in one clock cycle. As shown in Fig. 3, the 4-FFT processing module generates four beams pointed at angles of 0°, ±30° and ±90° (±90° beams are identical), respectively. The amplitude comparison DOA module uses two neighboring beams of the four-beam antenna array to receive the target signal simultaneously. The signal amplitudes received simultaneously from two neighboring beams are compared to obtain the power ratio of two adjacent beams, named differential beam (DB) as show in Fig. 3. The power of the DB corresponds to the DOA of the signal from a look-up table (LUT) of the amplitude comparison DOA module circuit. The power of the difference signal corresponds to the DOA of the signal from a target. The antenna patterns of two neighboring beams are expressed as follows. The main beam is (1). The auxiliary beam is either former neighbor beam

$$BF_A(\theta_{((s+1))_N}) = \sum_{n=0}^{N-1} x_n(m) e^{-jn\beta d \sin(\theta_{((s+1))_N})} \tag{2}$$

or latter neighbor beam

$$BF_A(\theta_{((s-1))_N}) = \sum_{n=0}^{N-1} x_n(m) e^{-jn\beta d \sin(\theta_{((s-1))_N})} \tag{3}$$

, where $((x))_N$ is represented as x modulo N. The antenna patterns of two neighboring beams represent that their spatial power spectrum can be designed with (1), (2), (3) and proper amplitude weightings. When a target is located at different directions between two neighboring beams, the power of the difference signal has a different value, which corresponds to DOA of the signal from a target. The DOA estimation of the amplitude comparison DOA mode depends on the difference in amplitude between two signals received simultaneously from two neighboring beams. In the amplitude comparison DOA module circuit, the signals from two adjacent beams, beam 1 and beam 2, are input to the divider where the small-value beam is selected as the numerator and the large-value beam is selected as the denominator to save one half of the dynamic range in the amplitude of the divider output. Because the DB curve is even symmetric in θ domain, only one half of ROM

memory is needed to store the values of DB LUT. The DOA LUT processing performs the comparison between the input DB value generated from the divider and the DB values stored in the LUT. The required processing time of the DOA LUT processing is 54 clocks per DOA estimation. The main merits of the proposed null steering beam-forming module, which consists of a complex multiplier and a complex adder, are its simple circuit and low computation load. The null steering beam-forming module combines linearly two adjacent beams of the DBF to form a null-steering beam $BF_{null}(\theta)$.

$$BF_{null}(\theta) = BF_M(\theta) + w(\theta)BF_A(\theta) \tag{4}$$

where the complex weight of the null-steering beam at the known DOA null angle θ_n is

$$w(\theta_n) = -\frac{BF_M(\theta_n)}{BF_A(\theta_n)} \tag{5}$$

According to the desired null angle, two adjacent beams $BF_i(\theta)$ and $BF_j(\theta)$ are chosen to generate the null beam $BF_{null}(\theta)$ using (4), (5) and following formula.

$$\begin{cases} BF_M(\theta) = BF_i(\theta) \\ BF_A(\theta) = BF_j(\theta) \end{cases}, \text{for} \left|\theta_n - \theta_i\right| < \left|\theta_n - \theta_j\right| \tag{6}$$

The complex weights of the null steering beam-forming module are pre-calculated and stored in the ROM. The required processing time of the null steering beam-forming module is one clock.

4. Experimental Results

The test results mode-switching function that the SDR multi-mode DBF processes the SAR echo signal at 0° angles in conjunction with high-power sinusoid interference at the angle of 10° are shown in Fig. 4, where ten short testing OFDM symbols are QPSK-modulated signals and constructed using a 64-IFFT. The first 64 sample outputs of the SDR multi-mode DBF, which are generated from the steering 0° beam-forming output of the multi-beam steering mode, are distorted due to a high-power interference at the direction of 10°. The DOA estimation mode is initiated and determines the direction of the interference signal i.e. DOA null angle θ_n. The outputs of the SDR multi-mode DBF in the sampled intervals between 66 and 130 are correctly spatial filtered by the null-steering mode. The steering multiple-beam, DOA estimation and null steering modes take up the processing time of 0.033μsec, 1.833μsec and 0.066μsec, respectively, which are less then the cross-range sampling time 40.36μsec of the SAR receiver. The proposed SDR DBF system meets the requirement of real-time processing. There are 96 18x18 multipliers and 28672 LUTs in the Xilinx Virtex II XC2V3000 FPGA with the clock rate 10MHz, of which hardware realization of the 4-FFT multiple beam-forming, amplitude comparison DOA, null-steering beam-forming modules and control circuit take up 64 (67%) and 8804 (28%), 5 (5%) and 3889 (14%), 4 (4%) and 224 (1%), and 0 (0%) and 504 (2%) 18x18 multipliers and LUTs, respectively.

5. Conclusions

The multi-mode DBF realized on the SDR platform, where the modularized processing modules are implemented using the FPGA processor, can reuse common modules for different modes to reduce the size and power consumption by a significant amount through hardware reconfiguration for the micro-satellite SAR. The required processing time for each of DBF modes is much less than the cross-range sampling time of the micro-satellite SAR. Due to the SDR approach, the proposed SDR DBF may add new modes or modify system parameters for the developed micro-satellite SAR without changing the hardware of the SDR platform.

References

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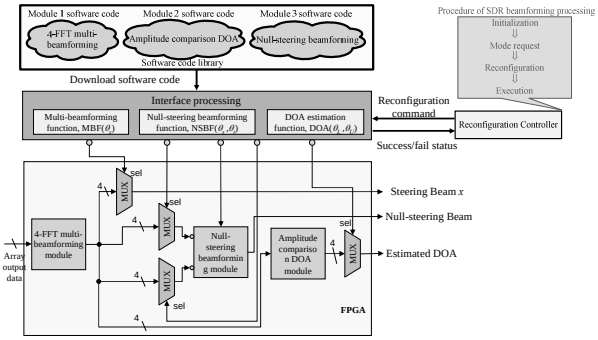

Figure 1: Hierarchical structure of the multi-mode DBF for the SDR reconfiguration

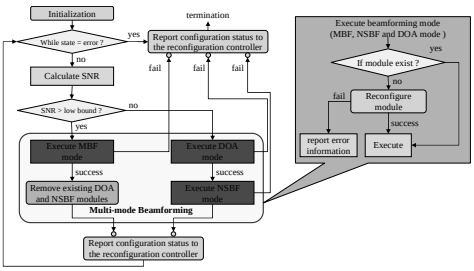

Figure 2: Flow chart of reconfiguration control algorithm of the SDR DBF

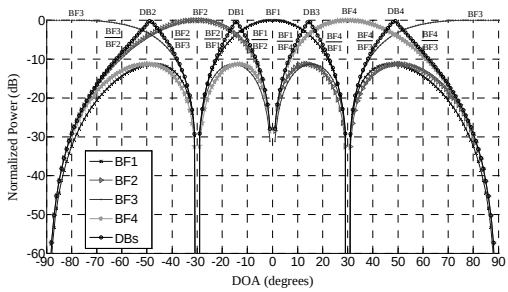

Figure 3: Four-element array yields 4 beams and 4 differential beams to cover the 180° in azimuth

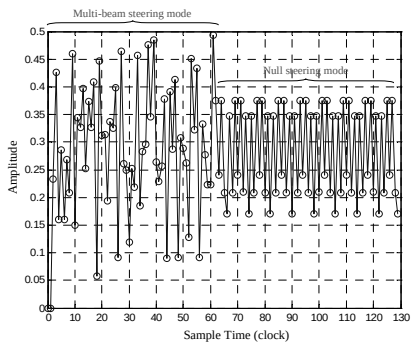

Figure 4: Test result of mode switching function