

High Spatial Resolution On-chip Active Magnetic Field Probe for IC Chip-Level Near Field Measurements

Y. Shigeta, N. Sato, K. Arai, M. Yamaguchi
Graduate School of Engineering
Tohoku University
Sendai, Japan
{shigeta, k-arai, yamaguti}@ecei.tohoku.ac.jp

S. Kageyama
Toppan Technical Design Center Co., Ltd.
Tokyo, Japan

shingo.kageyama@toppan.co.jp

Abstract— An on chip active magnetic field probe has been developed for IC chip-level magnetic near field measurements. A low noise amplifier (LNA) and a loop coil were implemented in 0.18 μm Si-CMOS technology, and solder-bonded to PCB to complete the probe. Its gain is 13.3 dB at 2 GHz. The probe is applied for magnetic near field evaluation of a test element group (TEG) chip that emulates Long Term Evolution (LTE) –class radio frequency integrated circuit (RFIC) receiver. It is demonstrated to detect on-chip in-band interference sources.

Keywords— magnetic near field measurement; magnetic field probe; low noise amplifier; LTE-class receiver

I. INTRODUCTION

Recent strong need for high frequency and high spatial resolution magnetic-field probes is pushed forward by the ever-higher speed and complexity of the electronic devices and systems, which directs toward investigating the causes of problems, and confirming the appropriateness of designs and countermeasure in terms of electromagnetic compatibility (EMC) [1].

The miniaturized shielded-loop probe is a known probe used to measure the distribution of the magnetic near-field of a large-scale integration (LSI) chip and a printed circuit board (PCB). A planar thin-film-type shielded-loop probe made by pattern plating is usable in the frequency range up to 7 GHz, and offers 10- μm class spatial resolution simultaneously [2]–[5].

Such a passive probe, however, is not sensitive enough to analyze the aggressor, propagation path, and victim of electromagnetic noise on IC chips because of the lack of sensitivity of a small loop. In this study, we have developed a magnetic-near-field probe consisting of an on-chip coil and an three-stage RF amplifier to achieve high spatial resolution and high sensitivity simultaneously. The probe performance is demonstrated on a test-element-group (TEG) chip which emulates a long-term-evolution (LTE)-class Si-CMOS RFIC receiver for the next-generation cell phone handsets

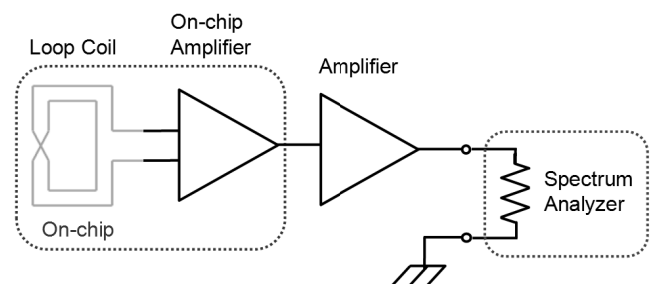


Fig. 1. Overall structure of the active probe.

II. ACTIVE MAGNETIC FIELD PROBE

Fig. 1 shows the overall structure of the active magnetic field probe. The chip is implemented with a coil and an amplifier at the tip of the active magnetic field probe. An impedance matching between the coil and the LNA on the chip is not provided as the impedance of the coil is as small as 12.8 ohms even at 10GHz, and the wire length between the coil and the chip is as short as 0.6mm. A high impedance amplifier receives the output signal from the coil. The magnetic near field is detected as the induced voltage on the loop coil. This voltage is amplified by the on-chip amplifier and the external amplifier connected at outside of the chip, then measured by a spectrum analyzer. In this work, the operating frequency range of the active magnetic field probe is set in 2 GHz band in order to analyze the noise in the LTE-class receiver circuit for the Band 1(2110 MHz-2170 MHz).

The coil and the circuit are implemented in a 0.18 μm CMOS image sensor (CIS) technology because of shuttle chip-fabrication scheme limitation, and the designable frequency band is limited below 1 GHz. Therefore, the targeting gain of the RF amplifier is set as 10 dB at 2 GHz.

A. Loop Coil

The 4 types of the coils are designed and fabricated on the test chip. Fig. 2 illustrates the loop coils as; (i) High signal to noise ratio type, (ii) Low resistance type, (iii) High induced

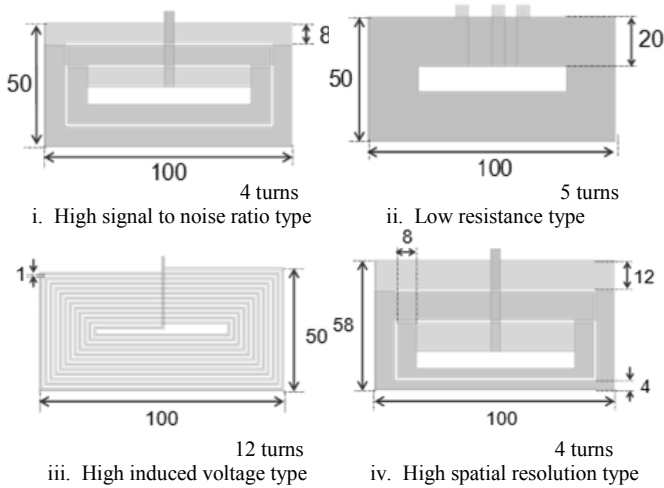


Fig. 2 General forms of the loop coils designed. (unit: μm)

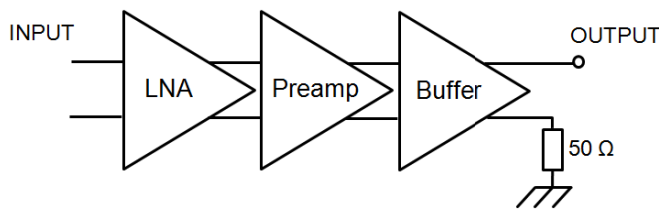


Fig. 3 On-chip amplifier

voltage type, and (iv) High spatial resolution type, respectively. All of coils are 100 μm wide, 50 μm long. These coils are featured by the number of windings and line width.

It is necessary to consider the signal to noise ratio (SNR) to detect low level flux voltage. The SNR is defined by,

$$SNR = 20 \log \frac{V_S}{V_N} \quad (1)$$

where V_N is the noise voltage and V_S is the signal voltage. V_N is determined by the thermal noise generated the resistance of the loop coil and the noise figure of on-chip amplifier. It is given by

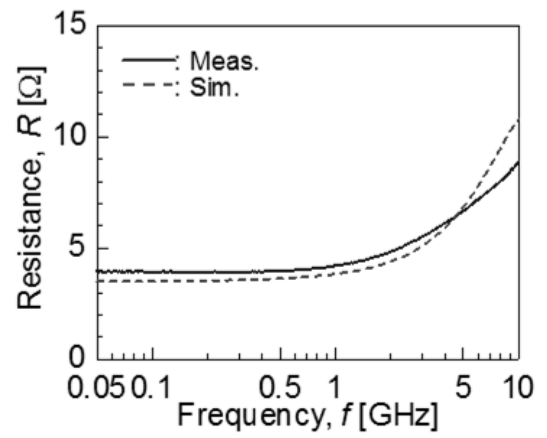
$$V_N = \sqrt{4P_N R} \quad (2)$$

where P_N [W] is the equivalent input noise level and R is the resistance of the loop coil. Therefore, V_N is proportional to the square root of the resistance of the loop coil.

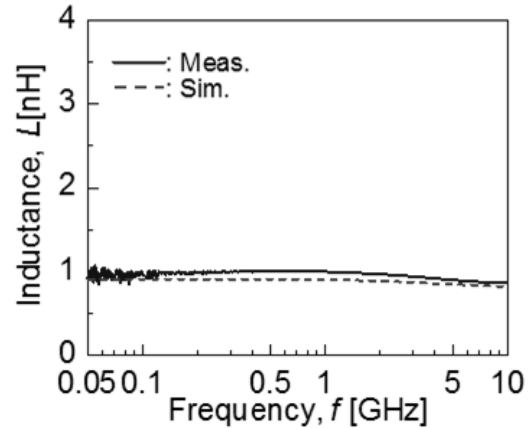
V_S is supposed to be down to 60 μV at 2 GHz, considering substrate coupling on chip and the shape and size of the loop coils. As a result, the expected resistance of the loop coil turned out to be lower than 11 Ω in order to obtain the SNR higher than 6 dB at 2 GHz. (1), (2).

B. On-chip Amplifier

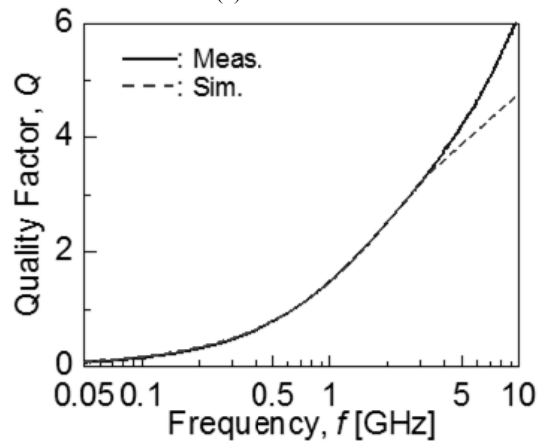
Fig. 3 shows the block diagram of the on chip amplifier. Three differential amplifiers connected in cascade are integrated on the test chip. A low noise amplifier (LNA) is set



(a) Resistance



(b) Inductance



(c) Quality Factor

Fig. 4 Electrical properties of the High signal to noise ratio type.

Table. 1 The result of electrical properties of the loop coils at 2 GHz.

	The type of loop coil				unit
	i	ii	iii	iv	
R	4.84	5.95	8.30	5.68	Ω
L	0.97	1.17	7.78	1.05	nH
Q	2.47	2.45	1.19	2.36	-

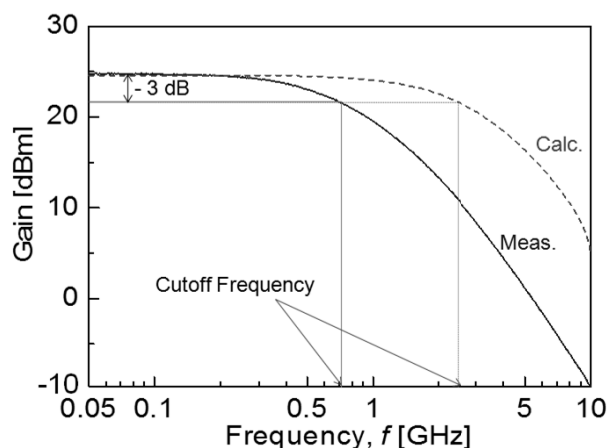


Fig. 5 Gain of on-chip amplifier

at the input stage to be sensitive to the low level signal from the loop coil. A pre-amplifier is connected at the second stage for further amplification. A single-ended output buffer is placed at the output stage for impedance matching to the systems impedance of 50Ω . The total gain of these amplifiers is 25 dB at lower frequency.

III. FUNDAMENTAL EVALUATION OF COIL AND AMPLIFIER

A. Loop Coil

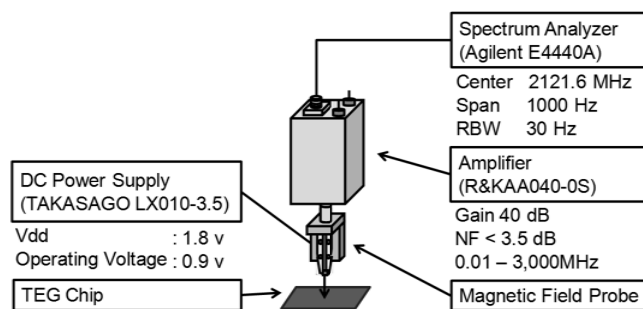
Electrical properties of the loop coils are evaluated by S-parameters on the chip using a vector network analyzer (VNA, N5244A Agilent Co.). S-parameter was transformed to Y and then to Z-parameters using π -type equivalent circuit model. The inductance, resistance and quality factor of the loop coils were derived from the Y-parameters. The parasitic resistance, inductance and capacitance of the lead wire are de-embedded using the Y and Z-parameters of reference circuit wiring patterns. Electromagnetic simulations have been carried out using a full wave FEM software (HFSS ver.11.1, Ansys Co.).

Fig. 4 shows electrical properties of the “High signal to noise ratio” type coil. Measured and simulated values agree well up to 3 GHz.

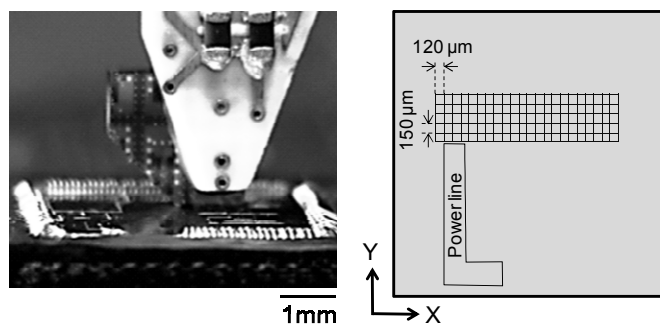
Table.1 shows electrical properties of 4 types of the coils. The resistance was lower than 11Ω for all of the coils, among which the “High signal to noise ratio” type coil exhibited the lowest resistance. Therefore this type is applied for the active magnetic field probe mounting, and used in the chapter IV.

B. On-chip Amplifier

The gain of the on-chip amplifier was measured using the VNA. The result was compared with the circuit simulation using SPICE (Virtuoso Spectre MMSIM ver.7.20.477.ISR16 Cadence Co.). Fig. 5 shows the gain of the on-chip amplifier. The measurement gain of 24.9 dB agrees with the simulation at lower frequency. At high frequencies the difference between the measurement and the simulation became noticeable. This is considered to be because of CIS process dedicated to low frequency applications. Nevertheless, the gain of on-chip amplifier still as high as 13.3 dB at 2 GHz, which meets the targeting gain.



(a) Magnetic field distribution on TEG chip.



(b) Active magnetic field probe above TEG chip.

(c) TEG chip.

Fig.6 Measurement of the magnetic field of TEG chip

IV. IC CHIP-LEVEL NOISE COUPLING MEASUREMENTS

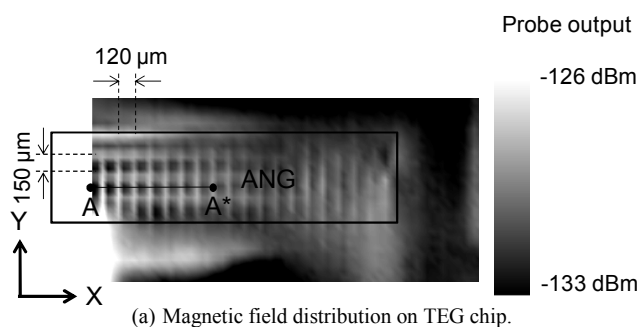
Magnetic near field of the TEG chip was measured by the active magnetic field probe and the 3-D near field scanner separately developed by us [9]. Fig. 6(b) shows a photograph of measurement. The PCB-mounted coil-amplifier chip is set closely to the surface of a bare-chip.

The TEG chip used in this work combines an arbitrary noise generator (ANG) for hardware emulation of RF noise coupling into the analogue receiver circuit chain of LTE-class RF IC for cellular phone handset on the same die[10]. The ANG mimics power noises in standard CMOS digital circuits and injects voltage variation into air and a silicon substrate of a chip.

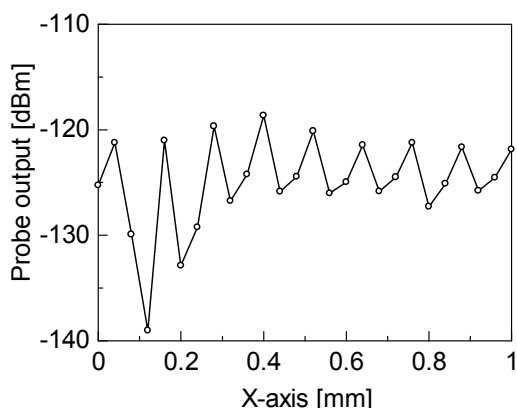
Fig. 6(c) shows a layout of TEG chip. The ANG emulates the true digital noise in the RF IC chip driven by a clock signal of 126.8 MHz, whose 17th harmonic of 2.1616 GHz conflicts with the LTE band 1 and becomes a potential source of the serious problem of desensitization

The probe output was evaluated by a spectrum analyzer (E4440A, Agilent Co.) through a low noise amplifier. The magnetic near field was measured in the X and Y direction, and these measuring pitches of $40 \mu\text{m}$. The magnetic field distribution of TEG chip was calculated from the root mean square of X and Y directions. The distance between the tip of the active magnetic field probe and the surface of TEG chip was $40 \mu\text{m}$.

Fig. 7 shows the results of magnetic field measurement of TEG chip. The shading was observed, the $120 \mu\text{m}$ pitch in X



(a) Magnetic field distribution on TEG chip.



(b) Probe output in the X direction at the line A-A*.

Fig. 7 Measurement results.

direction and the 150 μm pitch in Y direction. This result shows that the magnetic field generated from power-supply and return wirings of ANG was detected by the active magnetic field probe. Fig. 7(b) shows the probe output in the only X direction at line A-A* of Fig. 7(a). Measurement points of 40 μm pitch are the maximum value every 3 points (120 μm). This is also same for the Y direction (150 μm). The difference between the measurement values of 2 points was more than 6dB. This result shows that the spatial resolution of the active magnetic field probe is higher than 40 μm . The LTE receiver circuit on the TEG chip operated with the throughput fraction [11] more than 95% when the active magnetic field probe is put close to it. This means that the probe measurement and circuit operation are compatible to each other.

V. CONCLUSIONS

The test chip that integrates a loop coil and an RF amplifier was designed in CIS process and mounted to PCB by solder bump bonding to complete the magnetic near field probe. The gain of on-chip amplifier was 13.3 dB at 2GHz. The probe is applied to measure magnetic near field on the TEG that emulates LTE-class RF IC analogue receiver circuit chain and an arbitrary noise generator (ANG) for hardware emulation of RF noise coupling. The magnetic field generated from power-supply and return wirings inside the ANG was successfully detected.

These results demonstrate the usefulness of the developed active magnetic field probe.

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