

Parasitic Inductive Coupling of Integrated Circuits with their Environment

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Abstract—This paper describes an original methodology for the modeling of parasitic inductive couplings. The key idea is the use of magnetic hooks which are gates for magnetic fluxes that cross conductive loops and consequently induce parasitic voltages, thus disturbing the signal integrity. The multiple connected domains of integrated circuits are modeled by a Magneto-Electric-Equivalent-Circuit (MEEC), consisting of two mutual coupled circuits, an electric and magnetic one. Magnetic hooks are the externally connected nodes of the magnetic circuit.

Keywords—Chip; IC & Semiconductor EMC; Signal Integrity; Numerical Modeling; Computational Electromagnetics

I. INTRODUCTION AND PROBLEM FORMULATION

After observing the outstanding social importance of the nano-electronics, a steering European committee issued [1]. ‘More Moore’, ‘More than Moore’ and Design Automation are identified as central technology pillars that will underpin the future of the nano-electronics industry for the foreseeable future. Sustained downscale in the integrated circuits (IC) technology generate not only an incredible complexity of these systems, but also an increase of their running frequency. Many research projects aim to study subsequent effects, such as electromagnetic (EM) coupling (EM effects of noisy environment, substrate noise – internal IC coupling, etc.) in RF-IC blocks in the high frequency range; over 40 GHz. Advances described here are the result of the research project [2] whose main objective was to establish and to consolidate an effective bridge from layout to circuit in the RF-IC design. That means to develop new, efficient and accurate model extraction techniques in the way from Maxwell to Kirchhoff, which consists of three major steps: field problem formulation, numeric discretization and order reduction. The EM field problem is governed by Maxwell partial differential equations (PDE) with appropriate boundary conditions. Discrete, numerical non-compact model is described by a large system of differential-algebraic equations (DAE) and the goal is to obtain a reduced model, an equivalent compact circuit described by ordinary differential equations (ODE).

Proper boundary conditions are key aspects in the EM field problem formulation. The most appropriate for our needs seems to be the Electromagnetic Circuit Element (EMCE) boundary conditions (b.c.). These boundary conditions allow the compatibility and interconnection of devices having distributed parameters with any external circuit, solving so field-circuit coupled problems. In the simplest Electric Circuit Element (ECE) form of this b.c., disjoint surfaces S_1, S_2, \dots, S_m ,

called *electric terminals*, are identified on the boundary Σ of the computational domain Ω . In this case, there is no magnetic coupling between modeled device and its environment ($B_n=0$), electric currents cross the boundary only through terminals ($J_n=0$, in rest), each terminal being equipotential ($E_t=0$):

$$\mathbf{n} \cdot \text{curl } \mathbf{E} = 0 \text{ on } \Sigma; \mathbf{n} \cdot \text{curl } \mathbf{H} = 0 \text{ on } \Sigma \square S'; \mathbf{n} \wedge \mathbf{E} = 0 \text{ on } S', \quad (1)$$

where \mathbf{n} is the normal unitary vector, \mathbf{E} , \mathbf{H} are the electric and magnetic fields strength, S' is the union of electric terminals.

In the EMCE case, the magnetic coupling is allowed, but only through *magnetic terminals*: $S''_1, S''_2, \dots, S''_m$, their union being denoted by S'' :

$$\mathbf{n} \cdot \text{curl } \mathbf{E} = 0 \text{ on } \Sigma - S''; \quad \mathbf{n} \cdot \text{curl } \mathbf{H} = 0 \text{ on } \Sigma \square S'; \\ \mathbf{n} \times \mathbf{E} = 0 \text{ on } S'; \quad \mathbf{n} \times \mathbf{H} = 0 \text{ on } S''. \quad (2)$$

These new b.c. allow the coupling of the device with external electric as well magnetic circuits. Each terminal has two characteristic signals: current/flux and voltage, one being the input signal and the other being the output signal:

$$\text{El. terminal: } i_k(t) = \int_{\partial S'_k} \mathbf{H} \cdot d\mathbf{r}; \quad v_k(t) = \int_{C_k \subset \Sigma} \mathbf{E} \cdot d\mathbf{r}; \quad (3)$$

$$\text{Mg. terminal: } \varphi_k(t) = -\int_0^t \int_{\partial S''_k} \mathbf{E} \cdot d\mathbf{r} dt'; \quad v_{mk}(t) = \int_{C_k \subset \Sigma} \mathbf{H} \cdot d\mathbf{r}. \quad (4)$$

Although there is no theoretical difference between them, we will call the intentional terminals as “connectors” and the parasitic terminals as “hooks”. There are many fundamental consequences of EMCE boundary conditions: current and flux conservation as in Kirchhoff current/flux law (KC/FL); voltages law (KVL); expression of power transferred by the EMCE terminals; solution uniqueness theorem; as well as superposition theorems, thus resulting the operational form of the input-output relation, in the case of a hybrid-controlled, linear EMCE [3].

Considering a computational domains Ω with holes, it is obtained a more general concept of MEMCE (multiple connected EMCE). According to the Timotin’s theorem [4], the transferred power by these kinds of domains (Fig. 1) is:

$$p(t) = \sum_{k=1}^{m'-1} i_k v_k + \sum_{j=1}^{m''-1} v_{mj} \frac{d\varphi_j}{dt} + \sum_{s=1}^q (e_s f_s^0 - e_s^0 f_s), \quad (5)$$

Partial supported by ANCS-UEFISCDI Project PN-II-PT-PCCA-2011-3, no. 5/2012, monitored by Numerical Modeling Laboratory (LMN)

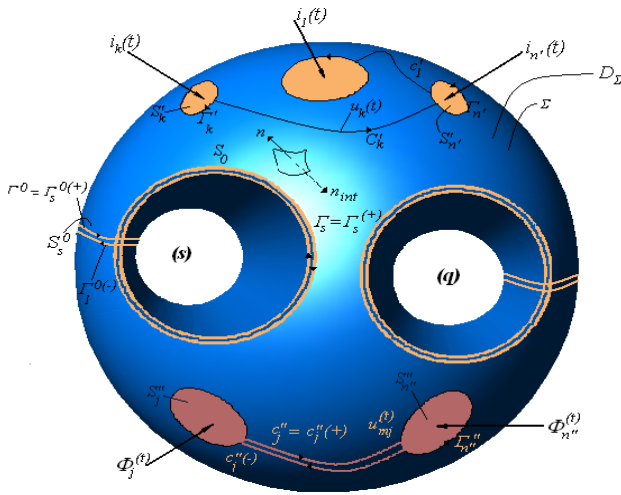


Fig. 1. Multiple connected Electromagnetic Circuit Element (MEMCE).

where the first term is related to the electric terminals, the second term is the power transferred by the magnetic terminals and the last term is related to the *tubular holes* of the computational domain.

Any tubular hole s may be removed, by the extension of Ω with a surface S_s , which cover the hole; or by an appropriate cut of Ω with a surface T_s . Therefore a hole introduces four signals, which describe the EM coupling:

$$\text{loop e.m.f./m.m.f.: } e_s = \int_{\partial S_s} \mathbf{E} \cdot d\mathbf{r}, \quad f_s = \int_{\partial S_s} \mathbf{H} \cdot d\mathbf{r}, \quad (6)$$

$$\text{cut e.m.f./m.m.f.: } e_s^0 = \int_{\partial T_s} \mathbf{E} \cdot d\mathbf{r}, \quad f_s^0 = \int_{\partial T_s} \mathbf{H} \cdot d\mathbf{r}. \quad (7)$$

The easiest way to describe the topology of Ω is by its graph and a tree/co-tree decomposition. Each co-tree branch generate a fundamental loop and by its cut is generated a fundamental cut-section.

II. NUMERICAL APPROACH

A. Principles of Finite Integrals Technique (FIT):

FIT is a numerical method to solve field problems, based on spatial discretization “without shape functions”, using [5]: dual staggered orthogonal grids, (Yee type = “complex of Cartesian cells”, nodes of secondary grid are in the centers of the primary grid cells), suitable for our Manhattan geometry; global variables as DOFs: voltages and fluxes on grid elements (faces, branches), and not local field components; global form of field equations (neither differential form as in FDTD, nor weak form as in FEM, nor integral equations as in BEM/MoM). The global field equations written on the mesh cells elements are called Maxwell Grid Equations (MGE). There is no numerical error in these fundamental equations, discretization errors being transferred to the constitutive relations. MGE are metric-free, sparse, mimetic and conservative system of DAE, without spurious modes:

$$\begin{aligned} \left\{ \begin{array}{l} \text{curl} \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t} \\ \Rightarrow \text{div} \mathbf{B} = 0 \end{array} \right. &\Rightarrow \left\{ \begin{array}{l} \oint_{\partial S_k} \mathbf{E} d\mathbf{r} = -\int_{S_k'} \frac{\partial \mathbf{B}}{\partial t} d\mathbf{A} \\ \Rightarrow \oint_{\partial \Omega_k'} \mathbf{B} d\mathbf{A} = 0 \end{array} \right. \Rightarrow \left\{ \begin{array}{l} C_v = -\frac{d\varphi}{dt} \\ \Rightarrow \mathbf{D}' \varphi = 0 \end{array} \right. \\ \left\{ \begin{array}{l} \text{curl} \mathbf{H} = \mathbf{J}_t \\ \Rightarrow \text{div} \mathbf{D} = \rho \end{array} \right. &\Rightarrow \left\{ \begin{array}{l} \oint_{\partial S_k'} \mathbf{H} d\mathbf{r} = \int_{S_k} \mathbf{J}_t d\mathbf{A} \\ \Rightarrow \oint_{\partial \Omega_k'} \mathbf{D} d\mathbf{A} = \int_{\Omega_k'} \rho dv \end{array} \right. \Rightarrow \left\{ \begin{array}{l} C' \mathbf{u} = \mathbf{i} + \frac{d\psi}{dt} \\ \Rightarrow \mathbf{D}\psi = \mathbf{q} \end{array} \right. \\ \Rightarrow \text{div} \mathbf{J} = -\frac{\partial \rho}{\partial t} &\Rightarrow \Downarrow \oint_{\partial \Omega_k'} \mathbf{J} d\mathbf{A} = -\int_{\Omega_k'} \frac{\partial \rho}{\partial t} dv \Rightarrow \mathbf{D}\mathbf{i} = -\frac{d\mathbf{q}}{dt} \\ \mathbf{J}_t = \mathbf{J} + \frac{\partial \mathbf{D}}{\partial t}. & \quad (8-13) \end{aligned}$$

Hodge operators describe material behavior, linking quantities defined on faces and dual branches.

$$\begin{cases} \mathbf{J} = \sigma \mathbf{E} \Rightarrow \mathbf{i} = \mathbf{M}_\sigma \mathbf{u} \\ \mathbf{D} = \epsilon \mathbf{E} \Rightarrow \psi = \mathbf{M}_\epsilon \mathbf{u} \\ \mathbf{H} = \nu \mathbf{B} \Rightarrow \mathbf{u}_m = \mathbf{M}_\nu \varphi \end{cases} \quad (14-16)$$

These operators are metric-dependent and they hold the discretization error. Classical FIT = MGE + Hodge (extracted from uniform field in each cell) must be improved and adapted, in order to achieve the requirements of the nowadays IC designers. We did it by domain partitioning (DP).

B. Local Magneto-Electric-Equivalent Circuit (MEEC)

Discrete form of Hodge operators (14-16) are the constitutive relations of two circuits: an electric one and a magnetic one, whereas MGE (8-10,12) are the general form of Kirchhoff equations of these circuits, which are coupled by means of voltage sources, controlled in current (actually in time derivative of magnetic flux, in the case of electric circuit). The graphs of these circuits are the two staggered discretization grids (Fig. 2).

C. State Space Models based on FIT

The MEEC equations, generated by FIT can be written as:

$$\begin{bmatrix} \mathbf{C}_e & \mathbf{0} \\ \mathbf{0} & \mathbf{G}_m \end{bmatrix} \frac{d}{dt} \begin{bmatrix} \mathbf{u}_e \\ \mathbf{u}_m \end{bmatrix} + \begin{bmatrix} \mathbf{G}_e & -\mathbf{B}' \\ \mathbf{B} & \mathbf{0} \end{bmatrix} \begin{bmatrix} \mathbf{u}_e \\ \mathbf{u}_m \end{bmatrix} = \mathbf{0}, \quad (21)$$

conducting to the standard descriptor, (semi)state equations:

$$\mathbf{C} \frac{d\mathbf{x}(t)}{dt} + \mathbf{G}\mathbf{x}(t) = \mathbf{B}\mathbf{u}(t); \quad \mathbf{y}(t) = \mathbf{L}\mathbf{x}(t), \quad (22)$$

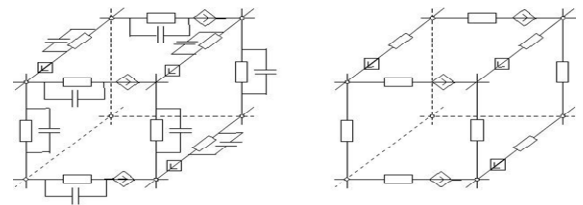


Fig. 2. Local Magneto(right)-Electro(left)-Equivalent-Circuits (MEEC)

if the discrete form of the EMCE boundary conditions are added [6]. Thus a Multiple-Inputs-Multiple-Outputs (MIMO) dynamic system is identified. The state variables x are the electric and magnetic voltages along the branches of primary and secondary FIT grids, respectively, augmented with the vector of output quantities y . Each floating terminal has a pair of input/output signals: current/flux or voltage, depending on excitation type.

III. MODEL ORDER REDUCTION

A. AFS-VF algorithm

There are many approaches and techniques to reduce the order of the model. According our experience, one of the most efficient methods to reduce the order of RF-IC models is based on Vector Fitting (VF) [7]. VF starts from the values of the transfer function, computed from (22) in a set of given frequency samples and it finds the best rational approximation of this frequency characteristic. For the problems we consider, there is no prior knowledge of these frequency characteristic samples. That is why a method to generate an optimal list of samples, by Adaptive Frequency Sampling (AFS), aiming to minimize the approximation error and to reduce the computational effort was implemented and tested on multiprocessor computers. Thus, a robust and efficient reduction procedure, called AFS-VF was obtained [8].

B. Domain Decomposition (DD) and Partitioning (DP)

The most expensive step of the MOR is the solving for several frequency samples, of the linear systems of complex equations $(j\omega\mathbf{C} + \mathbf{G})\mathbf{x} = \mathbf{B}\mathbf{u}$, aiming to compute the transfer function. Therefore an efficient technique to reduce the MOR computational effort is to decrease the number of frequency samples, as is done in AFS-VF. Another solution is to diminish the system size, without treating the accuracy. For this reason, the computational domain is partitioned in several sub-domains, each having a different regime of electromagnetic field. A typical IC is vertically partitioned as in Fig. 3, with:

- Electro-quasi-static (EQS) in Si substrate;
- Electro-static (ES) and magneto-static (MS) in air;
- Nonlinear drift-diffusion (DD) in active components;
- Full-wave (FW) in SiO_2 ;
- Magneto-quasi-static (MQS) in metallic conductors;
- Transmission-line (TL) equations in long interconnects.

Each subdomain is an EMCE, interconnected by terminals. The thin SiO_2 layer in which metal traces are embedded is horizontally partitioned as a puzzle in components, according to the design schematics.

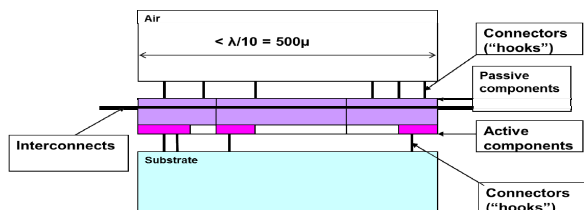


Fig. 3. Vertical partitioning of ICs.

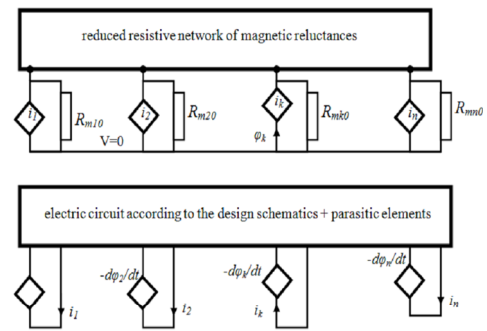


Fig. 4. The global, reduced MEEC model of IC.

Domain Decomposition (DD) is often used as the method to solve large problems iteratively on parallel computers. In DD, the continuity conditions are satisfied by field components: \mathbf{E}_p , \mathbf{H}_p , B_n and J_n on the interfaces between subdomains, meaning Dirichlet and Neumann for both electric and magnetic fields [9]. Discrete forms of these interface conditions are applied for all grid nodes placed on interfaces. Therefore each interface node is a terminal, and in DD interfaces are transparent for the EM field. In DP the interface conditions are approximated as in EMCE b.c., for each subdomain and the interface surfaces are no longer perfectly transparent for the field. In compensation, the number of interconnection terminals is much lower than in DD, nodes with close potentials being clustered. Moreover, the subdomains may be independently modeled and therefore iterations are no longer needed. Thus DP is a terminal reduction procedure, optimal hooks identification is its success key. In DP order reduction is done not only by terminal reduction, but also by grid calibration, hierarchical structuring, and by MEEC elements removing; in several field regimes, remaining only RC (in EQS), C(ES), R_m (MS), RR_m (MQS).

C. Global MEEC model

After the independent analysis and order reduction of all sub-domains, the extracted models are interconnected, generating the global magneto-electric circuit model. Unfortunately, since union of simple connected sub-domains is not always simple connected, the multiple connected domains should be treated carefully. It is the frequent case of circuits, which contain mesh holes (due to internal puzzle pieces that are missing). According to (5) these holes generate additional interactions, due to parasitic voltages, induced by magnetic fluxes passing through these holes, in the surrounded circuit loops. To model them, we place a magnetic hook in the hole of each fundamental loop of the electric circuit. The electric induced voltages are modeled by voltage sources placed in the co-tree branches of the electric circuit, sources controlled by the time derivative of the magnetic circuit "currents" (actually magnetic fluxes). Therefore, the global MEEC model has two circuits, coupled by controlled sources, as in Fig. 4. The topology of magnetic circuit of subdomains with MS field is a complete graph, with resistive branches. Since scalar MS potential satisfies Laplace equation, magnetic permeances $\mathbf{G}'_m = \mu_0\mathbf{C}/\varepsilon_0$ can be rapid extracted with *FastCap* [10]. Global MEEC is a sparse, reduced version of the local MEEC. The magnetic circuit has magnetic hooks as nodes. In

addition to the nodes generated by IC meshes, other *magnetic hooks are placed on the air/package boundary, aiming to describe the inductive coupling with environment.*

IV. RESULTS AND VALIDATION

In this section we will consider an example, which refers to a multiple connected conductor placed in air, over a Si substrate (its shape is as in Fig. 6 - up). It is included in a 3D rectangular box and the two ends of the conductor that touch the boundary are electric terminals, one grounded, and the other voltage excited. The box faces placed parallel to the conductor plane are magnetic hooks. The reference solution is the conductor impedance, computed by solving with FIT, in the EMCE box the Maxwell's equations. A tree comprising the three internal branches of conductor generates three independent loops that are the circuit meshes, which correspond in this simple case with the three internal magnetic hooks. In order to characterize the inductive effects, the MS field distribution was numerically computed in half of the computational domain, with Dirichlet boundary condition on hooks. Then the terminal magnetic conductance (permeance) matrix \mathbf{G}'_m of size 4×4 is obtained. Figs 5-6 show the MEEC model, which is perfectly equivalent with the RL model of conductor, if the magnetic noise V_n is missing.

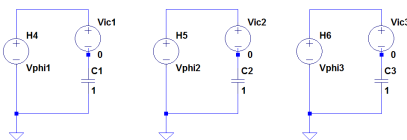


Fig. 5. Simple test case: Derivation circuit, circuit component of MEEC.

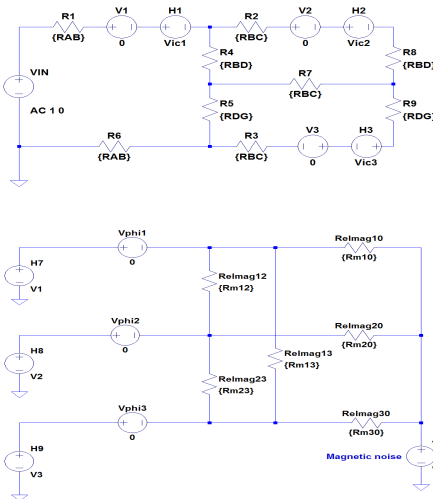


Fig. 6. Simple test case - component of MEEC: Electric circuit (up), Magnetic circuit (down).

The relative error at low frequency between the simulation of this circuit and the simulation for the whole 3D domain with full wave (FW) field computed with FIT was only 0.6 %. This result validates the proposed approach and it reveals also the efficiency of MEEC. The presented procedure can be easily

generalized for other conductor shapes, for which MEEC model can be extracted automatically, from layout. Moreover, each component may have its own parasitic model. More details and other validation tests are presented in [11].

V. CONCLUSIONS

Magnetic fluxes passing through loops of integrated circuits are sources of parasitic induced voltages. Multiple connected computational domains (as all circuits are) may be reduced to simple connected ones, by filling their holes (meshes). The natural way to identify these topology regularizations is to find a tree/co-tree decomposition of the circuit graph. Due to the fact that integrated circuits have their conductors embedded in a very thin layer, they can be considered as planar shells, having magnetic hooks placed over the circuit mesh holes. By using these hooks, a MEEC model may be automatically extracted, providing an efficient, accurate and robust modeling technique for inductive coupling of ICs with their EM environment.

Contrary to approaches based on partial inductances (such PEEC [12]), our DP/MEEC approach, based on meshes is robust, it has a solid theoretical base, and it enables the coupling with variable EM environments. Unlike PEEC and their variants, MEEC is able to characterize the susceptibility of modeled circuits to be influenced by external, parasitic, magnetic fields.

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