Power and Ground Phase Relation in LSI Power Distribution Network at Common-mode Noise Reduction

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***Abstract*—We derived expressions of power and ground voltage noises for reducing common-mode voltage in a power distribution network of an LSI and found that they have the same amplitude and a phase difference approaching 180°. To confirm this, we performed an experiment using a test board with a cover-metal structure-essentially, a floating conductor in an LSI package to reduce common-mode voltage. The evaluation was performed using an instrument that can measure the amplitude and phase difference of two channels in synchronization and calculate common-mode and differential-mode voltages. Results demonstrated phenomena similar to the expressions we derived.**

I. Introduction

In a power distribution network of an LSI, electromagnetic radiation is excited because of the LSI's high frequency current. In particular, a common-mode current, which flows in the power supply wiring and ground wiring in the same phase, brings about increased radiation. This radiation can cause malfunction in other instruments, so it is necessary to reduce the common-mode current.

We previously proposed a method to reduce common-mode noise [1] in which common-mode voltage is reduced by considering the parasitic capacitances between a printed circuit board (PCB) and a system ground. However, it's difficult to evaluate and predict the values of the parasitic capacitances because PCB has various structures and the distance to system ground is easy to change.

We therefore proposed another method using floating conductors [2]. When conductors covering an LSI package are used, parasitic capacitance in the package becomes stable. We can reduce the common-mode voltage by adjusting SMD inductors on both power and ground wirings. Although power supply and ground traces on PCB were shorted in high frequency by a bypass capacitor on PCB, there does exist a differential-mode voltage between power supply and ground. In the following section, we propose expressions to reduce common-mode voltage, including the inductance of the bypass capacitor, and derive the relation of power and ground voltages.

II. Reduction of Common-mode Noise Using Floating Conductor

An LSI power supply system composed of an LSI package, a printed circuit board (PCB), and a power supply cable is shown in Fig. 1(a). The package is connected to the PCB by inductors L_{V} and L_{G}. A floating conductor, which we call "cover metal", covers the LSI package. Parasitic capacitances C_{V} and C_{G} exist between the LSI package and this conductor. The values of these capacitances are stable even if the structure of the PCB changes. C_{BC} is a bypass capacitor on the PCB and L_{BC} is its parasitic inductance. When we consider a noise source as a current source, this circuit can be rearranged to the equivalent circuit in Fig. 1(b).

Next, we define the electrical potentials V_{Vpkg}, V_{Gpkg}, V_{V}, and V_{G} shown in Fig. 1(b). When the current on the cable is small and the frequency is high enough to regard the bypass capacitor on the package as inductive, V_{V} and V_{G} are derived as

$$V_{\mathrm{V}} = \frac{(L_{\mathrm{BC}} + L_{\mathrm{G}})V_{\mathrm{Vpkg}} + L_{\mathrm{V}}V_{\mathrm{Gpkg}}}{L_{\mathrm{V}} + L_{\mathrm{G}} + L_{\mathrm{BC}}}, \tag{1}$$

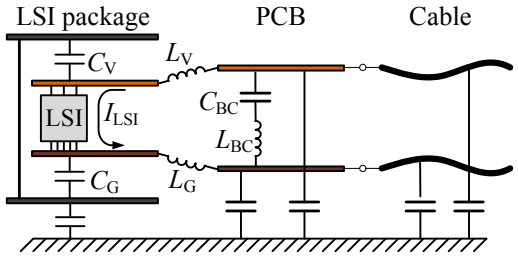
$$V_{\mathrm{G}} = \frac{L_{\mathrm{G}}V_{\mathrm{Vpkg}} + (L_{\mathrm{BC}} + L_{\mathrm{V}})V_{\mathrm{Gpkg}}}{L_{\mathrm{V}} + L_{\mathrm{G}} + L_{\mathrm{BC}}}. \tag{2}$$

Therefore, the common-mode voltage at the edge of the PCB is expressed as

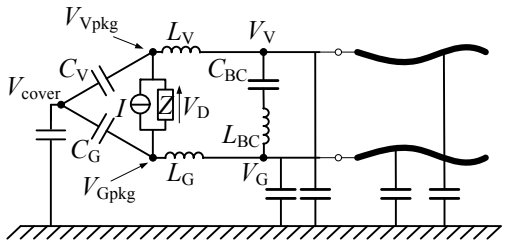
$$\begin{aligned} V_{\mathrm{C}} &= \frac{V_{\mathrm{V}} + V_{\mathrm{G}}}{2} \\ &= \frac{(L_{\mathrm{G}} + \frac{L_{\mathrm{BC}}}{2})V_{\mathrm{Vpkg}} + (L_{\mathrm{V}} + \frac{L_{\mathrm{BC}}}{2})V_{\mathrm{Gpkg}}}{L_{\mathrm{V}} + L_{\mathrm{G}} + L_{\mathrm{BC}}}. \end{aligned} \tag{3}$$

Under the condition that V_{cover}, which is the potential of the cover metal, is zero, the relation between V_{Vpkg} and V_{Gpkg} is, considering the path of the capacitors C_{V} and C_{G},

$$C_{\mathrm{V}}V_{\mathrm{Vpkg}} + C_{\mathrm{G}}V_{\mathrm{Gpkg}} = 0. \tag{4}$$



(a) Package with cover metal.



(b) Equivalent circuit.

Fig. 1. LSI power supply system.

Comparing the coefficients of V_{Vpkg} and V_{Gpkg} in Eq. (3) with those of Eq. (4), we derive a ratio for common-mode voltage to be zero, as

$$(L_{\mathrm{G}} + \frac{L_{\mathrm{BC}}}{2}) : (L_{\mathrm{V}} + \frac{L_{\mathrm{BC}}}{2}) = C_{\mathrm{V}} : C_{\mathrm{G}}. \tag{5}$$

The impedance balance condition is thus derived as

$$\frac{L_{\mathrm{V}} + \frac{L_{\mathrm{BC}}}{2}}{L_{\mathrm{G}} + \frac{L_{\mathrm{BC}}}{2}} = \frac{C_{\mathrm{G}}}{C_{\mathrm{V}}}. \tag{6}$$

When the condition shown in Eq. (6) is satisfied, the common-mode current that flows in the cable is not excited, and the relation between V_{V} and V_{G} becomes

$$V_{\mathrm{V}} + V_{\mathrm{G}} = 0. \tag{7}$$

This equation means that V_{V} and V_{G} have the same amplitude and the phase difference between them becomes 180°. Therefore, the amplitude of V_{C} is zero, as V_{V} and V_{G} cancel each other. We can therefore reduce the common-mode voltage in the LSI package with the cover metal by adjusting the value of L_{V} and L_{G} to satisfy Eq. (6).

III. Measurement on Test Board

We performed an experiment using a test board to observe the power and ground voltages under the condition that the common-mode voltage is reduced.

A. Test Board and Measurement Condition

The structure of the test board is shown in Fig. 2(a), 2(b), and 2(c). The package and the PCB both have two layers. The dielectric material is FR-4 ($\varepsilon_r = 4.25, \tan\delta = 0.02$) and the thickness of the board is 0.8 mm.

The package is 20 mm square and the area of its power plane (V_{DD}) is roughly equal to that of the ground plane (V_{SS}). A clock generator (Fox Electronics, FXO-HC536R-20) is placed on the top of the package as a noise source with an output frequency of 20 MHz. It has four terminals: V_{DD}, V_{SS}, E/D, and Output. The E/D terminal is connected to the power plane, so the status is enabled when the power voltage is supplied. The OUTPUT terminal is not connected with any plane or terminals. There is a 0.1-μF bypass capacitor between the power plane and the ground plane. Most of the bottom plane of the package is the cover metal, which is designed to have parasitic capacitance between itself and the top plane. In this experiment, the cover metal is placed only between the top plane of the package and the PCB for simplicity, but ideally both sides of the package should be covered so that the parasitic capacitance becomes more stable. We placed two 100-pF SMD capacitors C_{CV} and C_{CG} on the top of the package to be parallel with the parasitic capacitances between the package and the cover metal so that the capacitance ratio can be estimated more easily. Then, ignoring the inductances of the SMD capacitors, a relation of the capacitances in the package can be derived as

$$\frac{C_{\mathrm{G}}}{C_{\mathrm{V}}} = \frac{C_{\mathrm{CG}} + 12.0\ \mathrm{pF}}{C_{\mathrm{CV}} + 12.2\ \mathrm{pF}} \simeq 1, \tag{8}$$

where 12.2 pF is a parasitic capacitance between the power plane and the cover metal and 12.0 pF is that between the ground plane and the cover metal. These are calculated by three-dimensional electromagnetic analysis. SMD inductors L_{CV} and L_{CG} are placed on the top of the package, L_{CV} is placed on the power wiring, and L_{CG} is placed on the ground wiring. The package is mounted on the PCB by conductive pins, one from package power to PCB power and the other from package ground to PCB ground. This enables us to derive

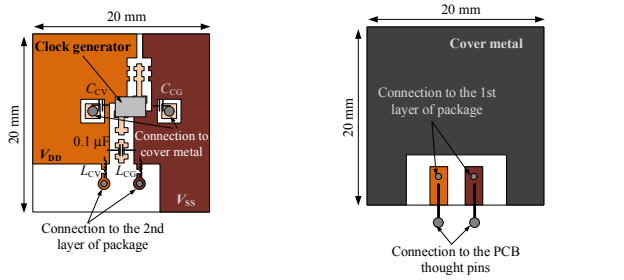
$$\frac{L_{\mathrm{V}}}{L_{\mathrm{G}}} = \frac{L_{\mathrm{CV}} + 2.27\ \mathrm{nH} + 0.25\ \mathrm{nH}}{L_{\mathrm{CG}} + 2.27\ \mathrm{nH} + 0.25\ \mathrm{nH}}, \tag{9}$$

where 2.72 nH is the inductance of the pins to mount the package on the PCB and 0.25 nH is half the parasitic inductance of two parallel bypass capacitors.

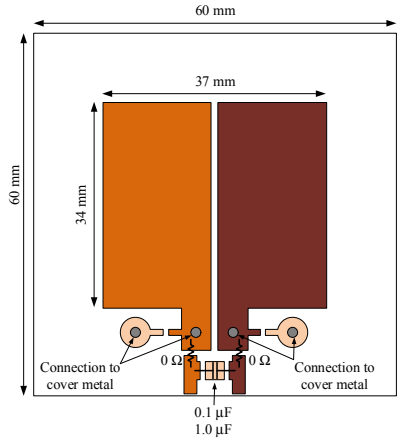
This PCB is 60 mm square, and the structure of the power plane and the ground plane at its top are symmetric. 1-μF and 0.1-μF bypass capacitors are placed in parallel. A floating conductor occupies all the space at the bottom plane of the PCB.

Arranging the values of L_{CV} and L_{CG} to satisfy $L_{\mathrm{V}}/L_{\mathrm{G}} = C_{\mathrm{G}}/C_{\mathrm{V}}$, we can reduce the common-mode voltage, and the common-mode current is therefore not excited to the cable. We supplied 3.3 V between the power and ground planes by a DC power supply device and used a Cross Domain Analyzer™(Advantest, U3872) as a measuring instrument. This instrument can measure the phase difference and amplitude of two signals in a frequency domain while obtaining phase synchronization. We calculated the common-mode voltage and differential-mode voltage between the power and ground wirings.

An equivalent circuit under this experiment condition was derived as shown in Fig. 3. We used the dual probe approach



(a) Top plane of package. (b) Bottom plane of package.



(c) Top plane of PCB.

Fig. 2. Structure of test package and PCB.

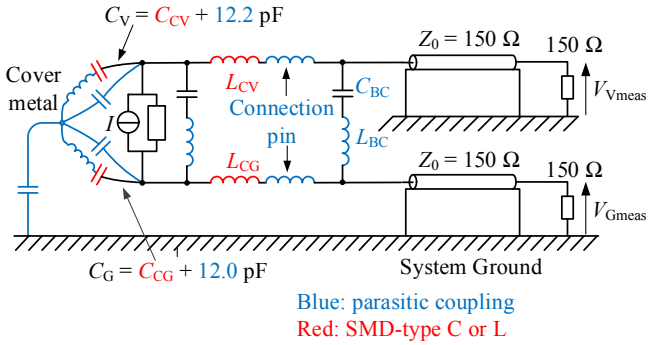


Fig. 3. Equivalent circuit of measuring system.

[3] with a work bench Faraday cage (WBFC) [4] as the measuring method. The input impedance of the power supply was 300 Ω and the system ground was an exterior wall of the WBFC.

B. Experimental results

Combinations of the L_{CV} and L_{CG} and L_V/L_G are shown in Table I. Results of the measurement are shown in Fig. 4. Only even number harmonics of oscillating frequency of the clock generator, which are dominant in power supply systems, are shown. The definitions of V_C and V_{dif} are shown in Eqs. (10) and (11). Both were calculated using the phase and the amplitude.

$$V_C \equiv \frac{V_{Vmeas} + V_{Gmeas}}{2}, \tag{10}$$

$$V_{dif} \equiv V_{Vmeas} - V_{Gmeas}. \tag{11}$$

TABLE I
COMBINATION OF INDUCTORS.

L_{CV} [nH]	10	15	12	18	47
L_{CG} [nH]	47	33	18	15	10
L_V/L_G	0.25	0.49	0.71	1.17	3.96

The power and ground voltages had about the same amplitude. Although there was a little deviation from the estimated C_G/C_V value, V_C was reduced by more than 10 dB at $L_V/L_G = 0.71$. Moreover, this reduction effect was obtained for all frequencies except 40 MHz, at which the amplitude of V_C was near the noise floor of 5 dBμV. The amplitude of V_{dif} did not differ significantly with changing L_V/L_G values. In addition, the amplitude of V_{dif} was large enough compared to the noise floor level. This indicates that the power plane and ground plane on the PCB had different potentials. However, as V_C approached the minimum point ($L_V/L_G = 0.71$), the phase difference between V_{Vmeas} and V_{Gmeas} approached 180°. Therefore, at the minimum point of V_C, V_{Vmeas} and V_{Gmeas} satisfied the condition shown in Eq. (7). We expected this result, since the impedance of the bypass capacitor on the PCB was lower than the input impedance of the power supply, which was 300 Ω (the sum of 150 Ω for the power-supply side and 150 Ω for the ground side). Therefore adjustment of impedance balance by changing L_{CV} and L_{CG} become available to reduce common-mode voltage. In fact, the impedance of the parallel bypass capacitors calculated with SPICE (Fig. 5) was sufficiently lower than 300 Ω, which means that values of L_{CV} and L_{CG} are dominant when it comes to reducing the common-mode voltage.

IV. CONCLUSION

We demonstrated through the equivalent circuit approach and experiments that, when common-mode voltage is reduced, the power supply and ground potentials have the same amplitude and the phase difference approaches 180°. The common-mode voltage was primarily reduced not by the amplitude but by the phase difference.

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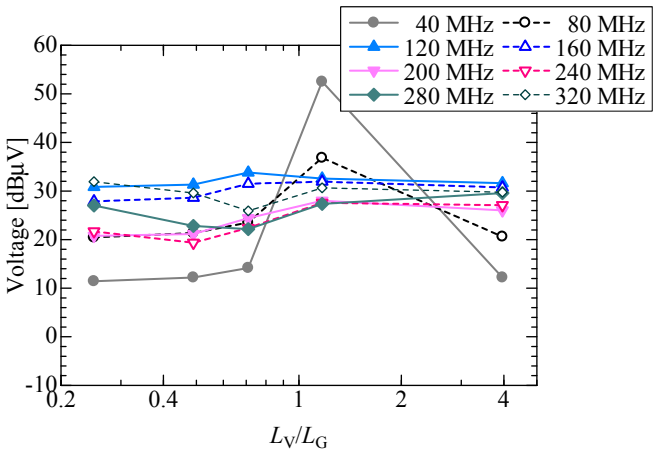
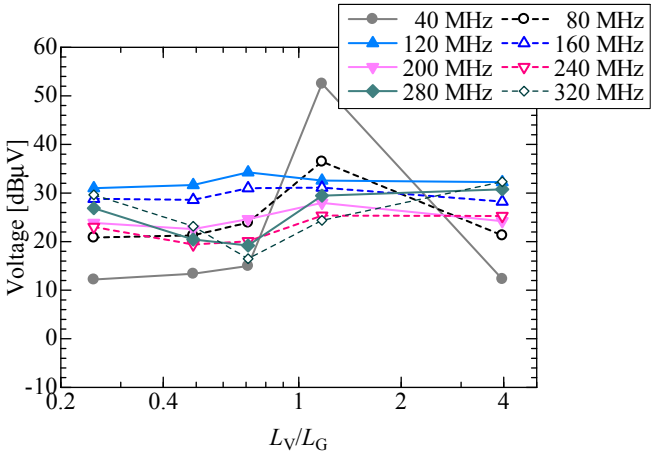
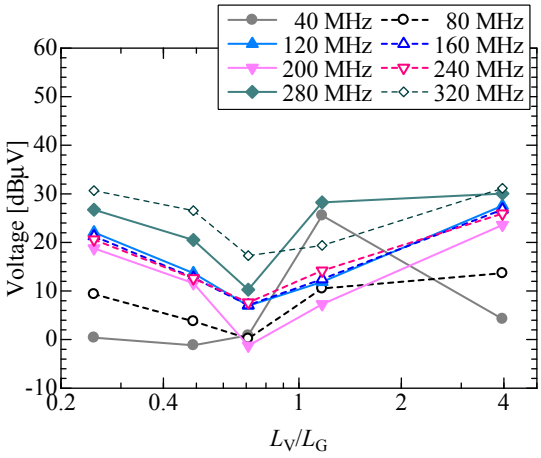


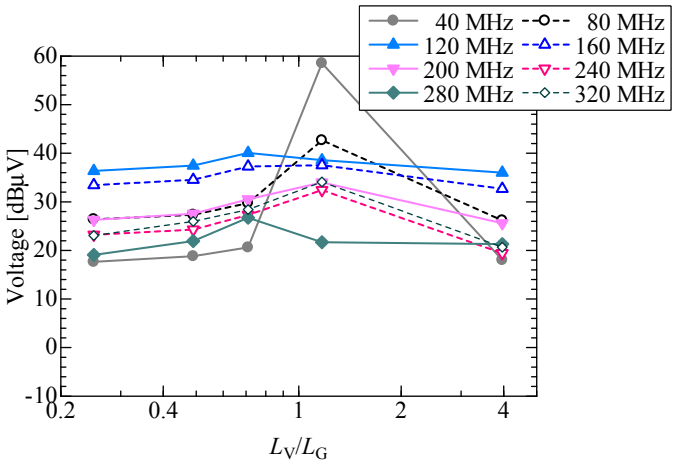
(a) V_{Vmeas} (amplitude).



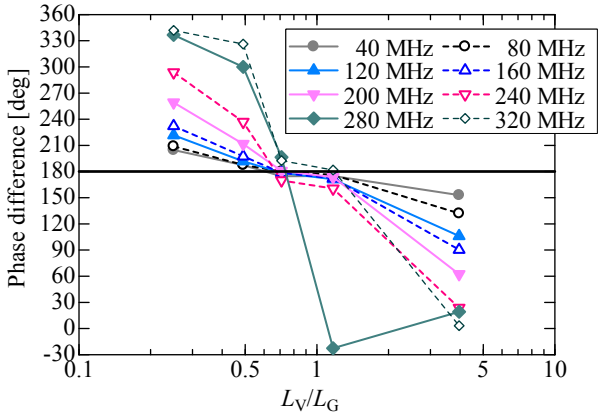
(b) V_{Gmeas} (amplitude).



(c) V_{c} (amplitude).



(d) V_{dif} (amplitude).



(e) Phase difference.

Fig. 4. Measurement results.

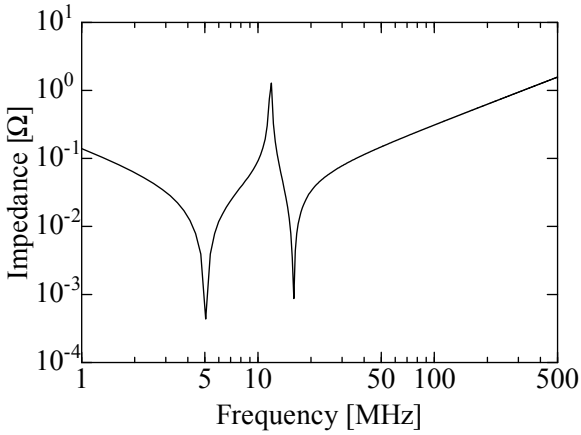


Fig. 5. Impedance of bypass capacitor.