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Optimize Transistor Size for FIR Pre-emphasis with Programmable Coefficients

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Abstract**—A finite impulse response (FIR) 6-tap pre-emphasis (PEP) filter with programmable coefficients was employed to counteract inter-symbol interface (ISI) in high speed backplane data communication or optical communication. The proposed circuit can operate at the data rates up to 10Gb/s. This circuit is designed in 90nm CMOS technology and operates at 1.0V. Simulation results show that the circuit improves signal eye diagram opening by at least 120mV at receiver end for the B mode channel from IEEE P802.3ap Task Force Channel Model Material. The total power consumption is 41.2mW for the whole pre-emphasis, including the retiming circuit and the pre-drive buffers**.

I. Introduction

Recently, the need to transport high volumes data from chip to chip or from board to board through backplanes while reduced I/O pin counts has replaced conventional low-speed parallel bus structure. A typical topology of a modular platform backplane is shown in Fig.1. It consists of two daughter boards, where the transceivers are located, and one backplane, which connects the two daughter boards. The daughter boards and backplane are attached by the connectors.

Due to the limited bandwidth of the channel, ISI is a major factor limiting the maximum distance and data rate in high speed SERDES communication. ISI is mainly caused by frequency dependent factors such as attenuation, phase propagation velocity (or group delay) of the backplane, and reflections found in interconnects, such as the connectors, PCB traces, and vias. Frequency dependent attenuation is mainly caused by the skin effect and dielectric loss of the backplane,

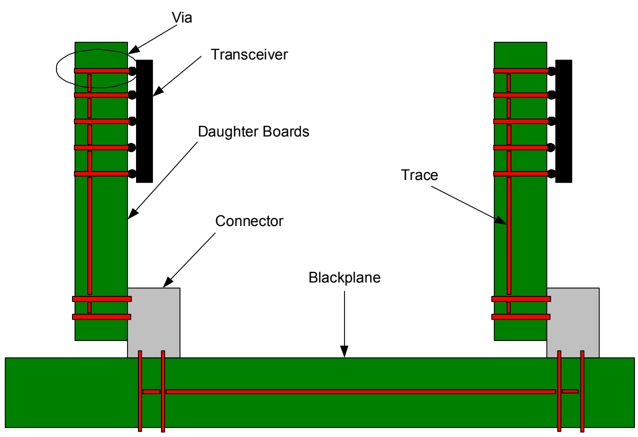


Fig. 1. Sample Backplane Topology

which suppresses high frequency content of the not-return-zero (NRZ) data stream and makes the output signal spread beyond one baud period. Frequency dependent group delay and reflection also distort the signals further. To counteract the ISI, a pre-emphasis in the transmitter side [1] or an equalizer in receiver side [2], or both [3], are employed. Finite impulse response (FIR) filters implemented in current mode circuit (CML) are the most popular circuits in pre-emphasis for the speed beyond 5Gb/s data communication. There are many types of equalizer, such as full response linear equalizer and partial response linear equalizer. To design an equalizer that can be operated as both types of equalizers requires a wide changing range (more than 10:1) for the second tap and the third tap. That means the current of the second tap and the third tap can be changed in a wide range. How to choose the transistors size to meet the wide range current changing is a challenge. In this paper, each tap of the pre-emphasis driver uses several pair of transistors instead of one pair of transistors, which is widely used in the traditional circuit. This paper is organized as follows. Section 2 describes the architecture of 6-tap FIR pre-emphasis. Section 3 describes detail circuit design using 90nm technology. Section 4 gives the simulation results for the selected channel. And finally, section 5 gives the conclusion.

II. Architecture of 5-Tap FIR Pre-emphasis

The mathematical expression of a FIR filter is [4]:

$$y(n) = \sum_{i=-N}^{M} C_i x(n-i) \tag{1}$$

where $\{C_i\}$ are the tap coefficients, N is the pre-tap, M is the post-tap, and C_0 is the main or reference tap. The proposed 6-tap FIR filter is 5 post-taps which means N=0 and M=5 in the Eq. (1). The optimized coefficients for specific channel, (e.g. simulated or measured S-parameters), are acquired from a MATLAB program, which has been developed as described in [5].

The architecture of the proposed FIR pre-emphasis is shown in the Fig. 2. It consists of the retiming circuit, the pre-driver with coefficient sign control, and the pre-emphasis driver with coefficient control. The retiming circuit consists of the DFFs. The sign of coefficients is controlled through the XOR gate with the data and the sign of the coefficients in the

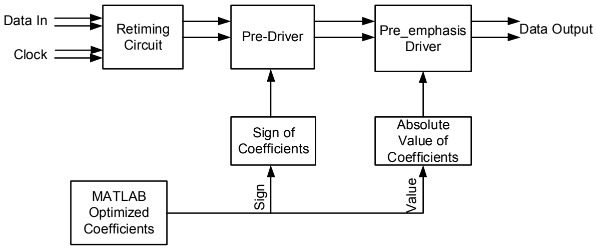


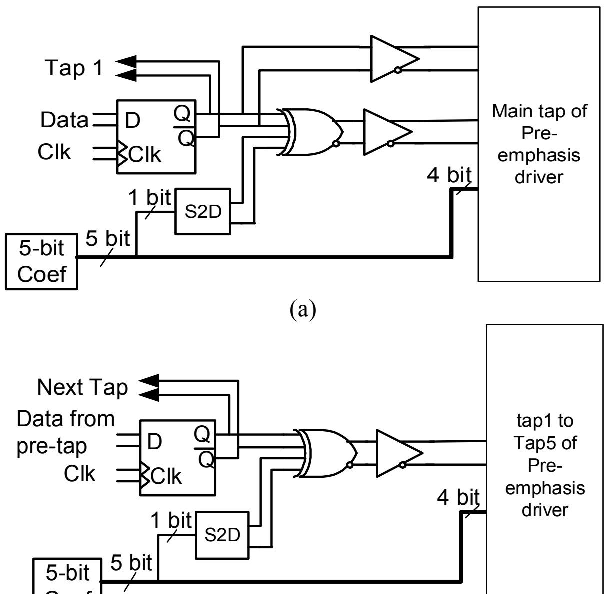
Fig. 2. Architecture of FIR Pre-Emphasis

pre-diver. The pre-driver also consists of buffers to drive large CMOS transistors in the pre-emphasis driver circuit. The absolute value of the coefficients controls the weight of each tap by controlling the tail current of the pre-emphasis driver through digital-analog converter current source (iDAC).

In this work, we select the channel mode B [6] as our application, which can be downloaded from IEEE P802.3ap Task Force Channel Mode Material.

III. CIRCUITS IMPLEMENTED IN 90NM TECHNOLOGY

Fig. 3 shows the circuit of the main tap and other taps (tap1 to tap5) of the FIR pre-emphasis. Given that the coefficients (loaded when the chip is initialized) do not change for a specific channel, circuits of registers that store the coefficients and single-to-differential (S2D) converters are implemented in rail-to-rail static CMOS circuits. This can save some power, because the static CMOS circuits consume less power compare to CML at low frequency. In this work, since the coefficients do not change after initialization, the power for S2D converters is very low, which is only the leakage current and very small and. All other circuits in Fig. 3 are implemented in CML circuits. Each tap consists of DFFs for retiming, an XOR for the coefficient's sign controlling, buffers to provide driving ability for pre-emphasis driver, a 5-bit iDAC that only uses 4-bit digital (we explain it late) to control the weight of each tap, and a 5-bit register to store the optimized value of coefficients (including the sign and value of the coefficients). The signs of



(a)

(b)

Fig. 3. Main tap (a) and other taps (b) of the FIR Pre-Emphasis

the coefficients are stored in the MSB. The coefficients values can be programmed through JTAG.

In order to save power, each DFF and XOR are optimized for power consumption according to their loads. For example, the loads for the DFF are one DFF for next stage and one XOR. So we do not need to design the high fan out, such as fan out 4. Design large fan out means heavy load and more power for the DFF. For the same reason, XOR is designed only for driving one buffer.

A. DFF, XOR and Buffer

The DFF consists of two D-Latches with a Master-Slave Structure. The transistor level circuits of D-Latch, XOR and Buffer are shown in Fig. 4. When the CMOS operates in saturation, the current is defined by the following equation:

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{OD})^2 \tag{2}$$

In order to reduce the size of the transistors, therefore reduce the input capacitor of the transistors, we select the minimum length for all transistors except the transistors used for the current mirror. Also all transistors in the circuit are transistors with low V_{th}. From the Eq. (2), we can see that for the same transistor size, the current is the ratio of square of the over-driver voltage, which is defined by $V_{OD} = V_{GS} - V_{th}$. If we use the low threshold voltage (V_{th}) transistors, the circuit can sense smaller V_{GS} compared to the regular V_{th} transistors and thus, the pair of transistors in CML can switch fully more easily.

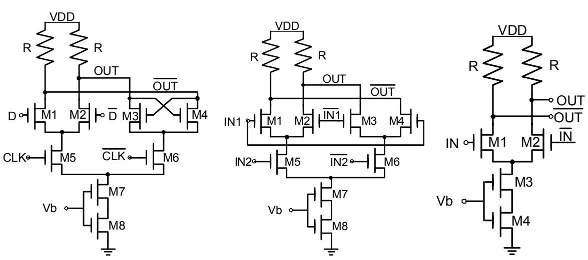
In general, with a CML circuit, more current results in faster operation. This is a basic trade-off between current, load resistance and capacitance [7]. Although we can not change the load resistance at the Pre-Emphasis driver, which has to match the channel impedance 50Ω, we can trade off current and load resistors for the D-latches, XORs and Buffers. For a given desired output swing v_o, the required transistors' size and current is given by (3) [7], and the slew rate is given by (4):

$$v_o = \sqrt{\frac{2I_{EE}}{\mu C_{OX}(W/L)}} \tag{3}$$

$$SR = \frac{I_{EE}}{C} \tag{4}$$

Here I_{EE} is the tail current of the CML circuit, C is the total capacitance of the output node.

So if we want the circuit to work faster, we need larger SR. That means the IEE should be larger. However, if we want to keep the same swing, we have to use larger transistors. That makes the capacitance become larger at the output node. We need to decide the output swing and slew rate to optimize the



(a) (b) (c)

Fig. 4. Schematic of D-Latch (a), XOR(b) and Buffer (c)

circuit to operate at the interested frequency. In our design, the output swing is 0.4V and the current of D-latch and XOR is 0.5mA. For the buffer and pre-emphasis driver circuit, the output swing is 0.5V.

Since the CML circuit is differential circuit, the common mode voltage also has to be set to an appropriate value. Otherwise, the circuit may not work. In our design, the common mode voltage chosen is 0.8V for DFFs, XORs, and 0.75V for pre-emphasis driver and final buffers that drive the pre-emphasis driver. The power supply in this design is 1.0V.

B. Pre-emphasis Driver

In high speed circuits design, the CMOS transistors are biased at maximum f_T, which gives us the current density around 0.28mA/µm [8]. Fig. 5 shows the simulation of the f_T for a 10µmx0.1µm NMOS transistor in 90nm technology. Fig. 6 shows one tap of the traditional pre-emphasis driver. As mentioned above, the current for one tap changes widely, so sizing the transistor to make the current density around the f_T is a challenge. For example if the maximum current for the specific tap is 10mA for a specific channel, but for another channel the maximum current is 1mA, if we choose size of the transistor to meet the maximum f_T according to the maximum possible current, which gives us the width of the transistor as 35.7µm and f_T as 129GHz. When the circuit operates for another channel, the current is 1mA and the current density is 0.028mA/µm, and the resulting f_T is 62.6GHz. If the current change is wider, the f_T drops more. Fig. 7 shows the proposed circuit of the main tap, which use several pair of transistors for one tap instead of one pair of transistors in the traditional circuit. One benefit of proposed circuit is that it reduces the input capacitance. Because in the proposed circuit, some transistors always turn off (C_i=0). Only the required transistors turn on and off depending on the data. In the traditional circuit, the big transistors always turn on and off. When the transistors turn on, they operate at triode region. When the transistors operate at turn off region, the C_{gs} and C_{gd} are both overlap capacitance C_{ov}, when the transistors operates at triode region, the C_{gs} and C_{gd} are both equal to $C_{gc}/2+C_{ov}$ (C_{gc} is gate to channel capacitance)[9]. Another benefit is that all current sources are identified with the same factors. All current sources are operated at the same current density, so all the voltages of the output of the current sources are the same (ignore the mismatch of processing and temperature), so the current are keep the same factors. In the traditional circuit, the current density of the driver depends on the coefficients value, so the voltage of the current source also dependent on the

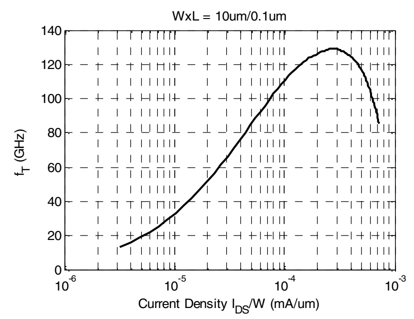


Fig. 5. f_T Vs. current density
NMOS WxL=10µmx0.1µm, 90nm technology

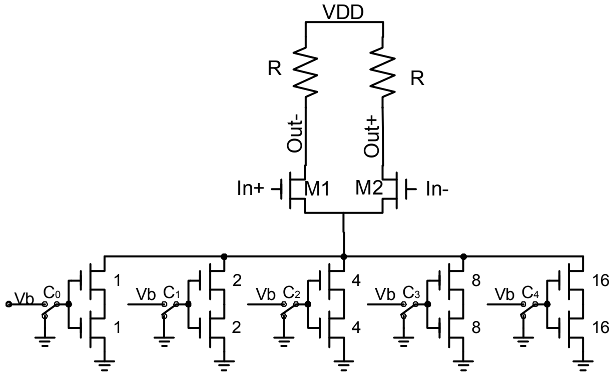


Fig. 6 Traditional circuit of one tap pre-emphasis driver

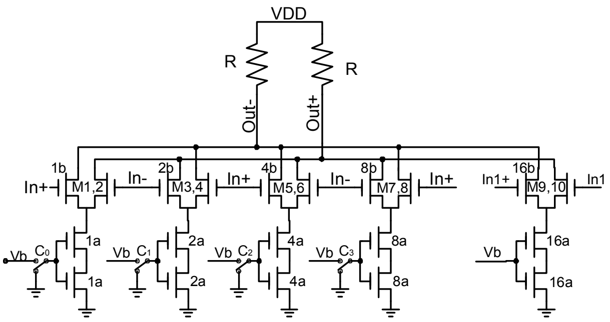


Fig. 7. Proposed circuit of main tap

coefficients values due to the limited impedance of the current source.

In order to match the channel impedance, the load resistors are 50Ω. For the DC coupling connection with a channel and receiver, the total load impedance is 50Ω//50Ω=25Ω. For most industry standards, the CML output swing is between 400mV to 600mV, which results in the output range from 800mV to 1.2V. In our design, we selected 1V for the output range, which makes the differential output changes from -0.5V to 0.5V. For CML the output voltage is given by [7]:

$$V_o = I \times R_{load} \tag{4}$$

To get 0.5V at output, the circuit needs 20mA current in total of the 5-bit digitally controlled current source. So for 1 LSB, the current is 0.625mA (20mA/32). If we use these parameters for the design, the maximum current of each tap is 20mA. From the optimized coefficients, we notice that the maximum current of each tap cannot be 20mA (in this case, the coefficients of other taps are zero). Also the maximum values of the coefficients of each tap are not the same. In our application, we decide that the maximum current values for each tap are 16mA, 8mA, 8mA, 4mA, 2mA, 2mA from main tap to tap5 respectively. We still use 5-bit digitally controlled current sources, and now 1 LSB is 0.5mA (16mA/32). This improves the absolute resolution of the iDAC from 0.625mA to 0.5mA using the same digital circuit. Only the main tap needs 5-bit digital and the sign of the coefficients of the main tap is always positive. We can use 4-bit iDAC and one fixed bit current source to implement 5-bit iDAC. The circuit of the main tap is shown in the Fig. 6 b). The input data of the 4-bit digital branches is the data of the main tap but can change the sign of the value through the XOR, the input of the fixed branch is directly driven by the data of main tap. So total the current of the main tap is defined by:

$$i_{main} = 16 I_{LSB} \pm I_{LSB} \sum_{0}^{3} C_i 2^i \qquad (5)$$

Here the I_{LSB} is the current value of 1 LSB. When the current of main tap is more than or equal to 16 I_{LSB} (8mA), the sign of the coefficient of main tap is positive. However, when the current of main tap is less than 8mA, the sign of the coefficient of the main tap is negative. So the current range of the main tap is I_{LSB} to 31 I_{LSB}, which is 0.5mA to 15.5mA. It only losses the zero current value compare to use 5-bit digital DAC current source, which should not happen for the main tap.

Fig. 8 shows other taps of the pre-emphasis driver. The number of branches depends on how many bits need for that tap according to the maximum current of this tap. The benefit of using different number of branches for each tap is reduce the total transistor size of the specific tap according to requiring, so it reduce the current of the pre-driver circuit, therefore it save the power of the circuit.

IV. SIMULATION RESULT

The channel used in the simulation was obtained from the IEEE 802.3 task force. We have chosen the channel B mode in our simulation. The test bench with the channel is shown in Fig. 9. The input data is PRBS15. At the receiver, we use 50Ω resistors connected to the power supply to replace the receiver.

Fig. 10 shows the impulse response (a) and SDD21(b) of the channel B1, B12 and B20. In order to compare the maximum of the impulse response, we plot the maximum value at the same time reference (time=0), ignore the delay of the channel. From the figure, we can see that channel B1 has a larger reflection at point A. The reason for this is that the channel is very short and the reflection has a short time from the peak value and less attenuation. For the B12 and B20, we should also see the reflection if we plot longer time of the impulse response. However the reflection should be smaller than that of B1, because the B12 and B20 have more attenuation than that of B1.

Fig. 11 shows the simulation results at transmitter (Tx) and receiver (Rx) for channels B12 with out pre-emphasis. From a) and b), it shows the eye of the transmitted signal opens more than 500mV but the received signal without FIR pre-emphasis is completely closed. From Fig. 11 a), we can see that the signal at Tx is not very clean, that is because the reflection from the channel distorts the signal. Fig. 12 shows the simulation results at Tx and Rx for different channels. For different channel the eye opening is different, the results are listed in Table 1. The results show that the vertical opening of the eye diagram of B1 (Fig. 12 b) is the largest and B20 (Fig. 12 f) is the smallest. This is because the attenuation of B1 is the smallest, about -10dB at 5GHz, and the attenuation of B20 is the largest, about -18dB at 5GHz (from Fig.10 b).

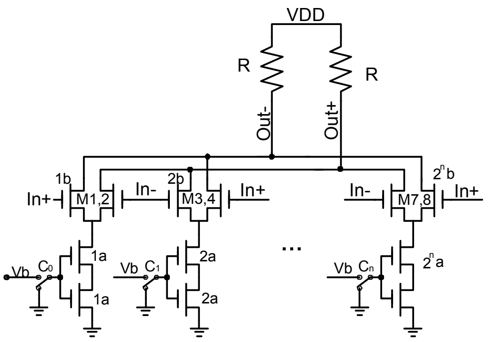


Fig. 8 Proposed circuit of other taps

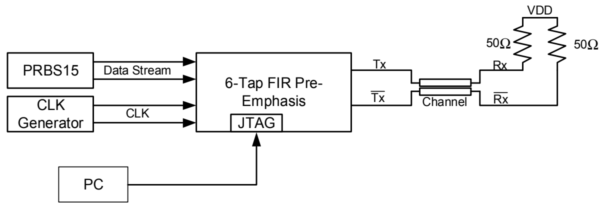
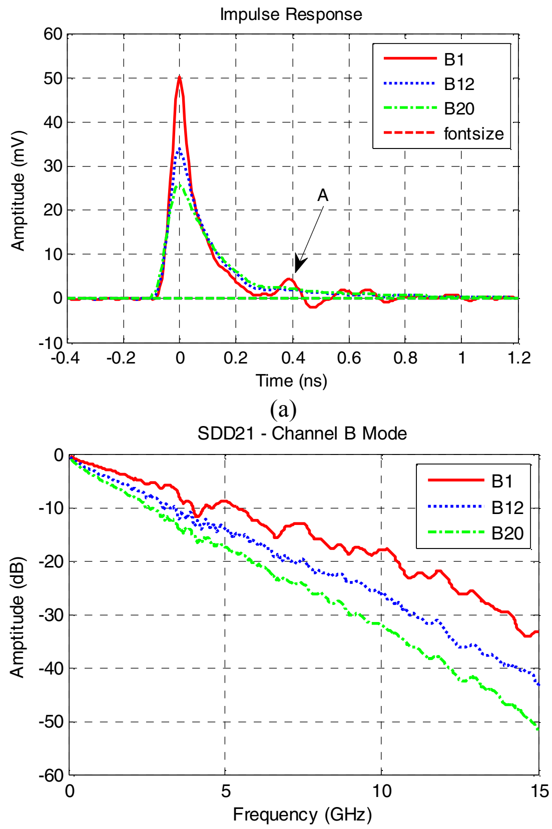


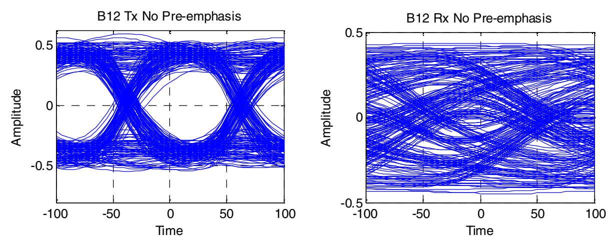
Fig. 9. Test Bench



(a)

(b)

Fig. 10. Impulse Response (a) and SDD21(b) of B Mode Channel



(a) (b)

Fig. 11. Eye Diagram of the signals transmitted and received for model channel B12 without PEP

(a)B12 Signal at Tx, No PEP (b)B12 Signal at Rx, No PEP

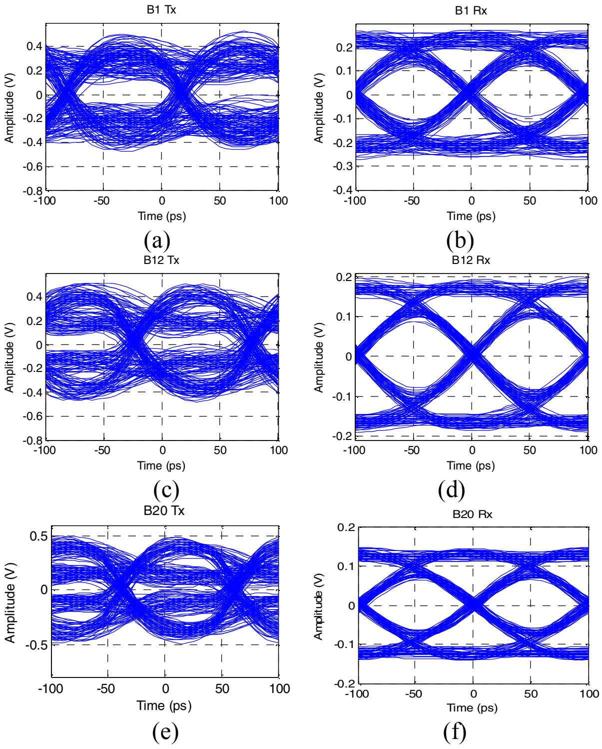


Fig. 11. Eye Diagram of the signals transmitted and received for model B channels
(a) B1 Signal at Tx, with PEP (b) B1 Signal at Rx, with PEP
(c) B12 Signal at Tx, with PEP (d) B12 Signal at Rx, with PEP
(e) B20 Signal at Tx, with PEP (f) B20 Signal at Rx, with PEP

The total current for the 6-tap FIR pre-emphasis is 41.2mA and consumes 41.2mW. The comparison of power dissipation is listed in the Table 2. From Table 2, we can see that the power dissipation is lower compared to other designs. Although the lowest power dissipation is the design in [13], this work has 4 more taps than that of the design in [13]

Table 1 Channel B Eye Opening

		B1	B12	B20
Eye Opening	Horizontal (UI)	0.7866	0.8225	0.8262
	Vertical (mV)	208.0	165.7	122.8

Table 2 Power dissipation comparison

	Taps	Tech-nology	Power (mW)	VDD (V)	Data Rate Gb/s
[1]	3		183.2		5/10
[3]	4	90nm	70	1.2/1.0	10
[10]	4	.13um	180	1.5	10
[12]	4	90nm	95	1.2	10
[13]	2	.18um	40.5	1.8	6
This work	6	90nm	41.2	1.0	10

V. Conclusion

A 6-tap programmable coefficient FIR pre-emphasis has been designed using 90nm technology. The tap coefficients, including the sign are completely programmable by changing the value of the registers through the JTAG interface. With the proposed circuit, a 10Gbp/s operation has been demonstrated over channel B mode backplane. Eye opening of all channels meets the specification of CEI 2.0 [14], which the minimum vertical opening is 100mV for CEI-11G-LR/MR and the minimum horizon opening is 0.475UI. The power dissipation is only 41.2mW at 1.0V power supply.

References

[1] C. H. Lin, S.J. Jou, "4/2 PAM Pre-emphasis Transmitter with combined driver and mux" in Proc. Asian Conference On Solid-State Circuits Conference. Pp189-192, Nov. 2005

[2] J.F. Bulzacchelli, et al "Power-Efficient Decision-Feedback Equalizers for Multi-Gb/s CMOS Links" in Proc. Conf. on Radio Frequency Integrated Circuits, pp 507-510, Jun. 3-5, 2007

[3] J.F. Bulzacchelli, et al "A 10-Gb/s 5-Tap DFE/4-TapFFE Transceiver in 90-nm CMOS Technology" IEEE J. Solid-State Circuits, Vol. 41, pp 2885-2900, 2006

[4] M. Li, T. Kwasniewski, et al "A 0.18-um CMOS transceiver design for high-speed backplane data communications" in Proc. Conf. On Circuits and System, pp 1158-1161, Vol.2 May 23-26, 2005

[5] M. Li, T. Kwasniewski, et al "FIR filter optimization as pre-emphasis of high-speed backplane data transmission" in Proc. Conf. On Communications, Circuits and Systems, PP 773-776, Vol.2, June 27-29, 2004

[6] W. Peters, IEEE P802.3ap Task Force Channel Model Material. http://grouper.ieee.org/groups/802/3/ap/public/channel_model/index.html

[7] John Rogers, Calvin Plett, Foster Dai, "Integrated Circuit Design for High-Speed Frequency Synthesis" Boston, Artech House, 2006

[8] D.O. Dickson, et, al "The Invariance of Characteristic Current Densities in Nanoscale MOSFETs and Its Impact on Algorithmic Design Methodologies and Design Porting of Si(Ge) (Bi)CMOS High-Speed Building Blocks" IEEE J. Solid-State Circuits, Vol. 41, pp 1830-1845, 2006

[9] Thomas H. Lee, "The Design of CMOS Radio-Frequency Integrated Circuits" Cambridge University Press, 1998

[10] F. Weiss, D. Kehrer, et al "Transmitter and Receiver circuits for serial data transmission over lossy copper channels for10Gbps in .13 um CMOS" in Proc. Conf. On Radio Frequency Integrated Circuits, June 11-13, 2006

[11] A. Healey, "Challenges and Solutions for Standards-Based Serial 10Gb/S Backplane Ethernet" in Proc. Conf. On Custom Integrated Circuits, pp 139-144, Sept. 17-19, 2007

[12] A. Rylyakov and S. Rylov, "A low power 10 Gb/s serial link transmitter in 90-nm CMOS" in Proc. Conf. On Compound Semiconductor Integrated Circuit Symposium. pp. 189–19, Oct. 30 – Nov.2, 2005

[13] C.M. Chu, C.H. Chuang, et al. "A 6Gb/s Serial link transmitter with pre-emphasis" in Proc. Conf. On VLSI Design, Automation and Test, pp.1-2, April 25-27, 2007

[14] OIF2005, "Common electrical I/O (CEI)- electrical and jitter interoperability agreements for 6G+ bps and 11G+ bps I/O" IA# OIF-CEI-02.0, 28th, Feb, 2005