A Monolithic 10-Gb/s CMOS Limiting Amplifier for Low Cost Optical Communication Systems

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Abstract— **In this paper, a 10-Gb/s limiting amplifier (LA) was implemented in 0.18μm CMOS. Modified active inductors and active feedback topology are employed to eliminate the trade-off among circuit bandwidth, power dissipation, and layout area, which is suitable for low cost applications. Based on the measurement results, the realized LA can operate up to 12-Gb/s with a 125mV_{pp} single-ended output through equivalent 25-Ω load. The input dynamic range is 40dB corresponding to the signal level range from 4mV to 400mV. The RMS jitter of the output signal is 2ps and the total power dissipation (including output buffer) is only 60mW under a supply of 1.8V.**

I. INTRODUCTION

The exponential growth of the internet and multimedia communications has greatly increased the demand for high speed communication systems. The optical communication systems are expected to play an important role in realizing the future multimedia communication.

Optical receivers operating at 10-Gb/s are widely used in optical access networks (OANs), backbone telecommunication networks and Ethernet fiber optic links which used for local area networks (LANs). Some high speed CMOS circuits with spiral inductor loads are realized, which consume large power or large die size [1]-[3]. However, low power dissipation compact chips are the first choice for commercial communication systems.

Shunt peaking (SP) technology is widely used to extend the bandwidth of gain stages, which can be realized by thick top metal spiral inductors, bonding wire inductors or compact active inductors. Although active inductors introduce a little bit larger noises and have smaller quality factors (Q), they consume much smaller chip area, which is still a good choice for low cost applications.

In this paper, a 10-Gb/s CMOS LA is presented, which uses active inductors and active feedback technique to boost the bandwidth, to reduce the power consumption and the die size simultaneously.

II. THE PHYSICS OF SHUNT PEAKING

The maximum speed of a common source amplifier is limited mainly by the parasitic capacitances of the transistors and the layout. The physics of shun peaking is quite straightforward. Since the voltage on parasitic capacitors or load capacitor is unable to change abruptly, at the very beginning the additional current is almost provided by capacitors only and the output voltage changes quickly. With the output voltage going down, the current provided by the load resistor will increase, but the current provided by capacitors will decrease. The addition of the inductor in series with the drain resistor delays the current flow through the branch containing the resistor, making more current available for charging the device capacitors, and reducing the rising and falling times. From another perspective, the addition of an inductance in series with the load capacitance introduces a zero in the transfer function of the common source stage which helps offset the roll-off due to parasitic capacitances [4]. In perfect world, inductive peaking can increase the bandwidth to about 1.72 times larger than the unpeaked case. Additionally, inductance values are scaled with the same factor as the drain resistors.

Both spiral inductors and bonding wire inductors are often used to implement shunt peaking. On one hand, additional pads and poor accuracy control for bond inductors are hardly acceptable for the required chip area and integration density. On the other hand, it is very difficult to realize a high-inductance and high-Q on-chip spiral inductor with a small layout area. Although high-Q values are not indispensable for shunt peaking inductors since the effective Q is determined by the poly-silicon load resistor that is connected in series to the shunt peaking inductor, high self-resonant frequency is necessary for high frequency operation. Fortunately, active inductors are compact and can work up to $f_T/2$ [5], which makes it the best candidate to be used as shunt peaking load.
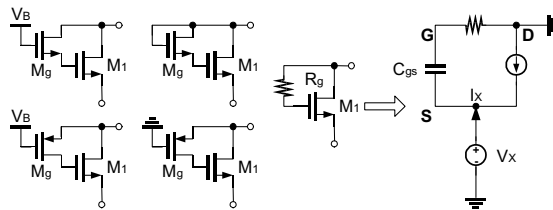

Fig. 1. Active inductors and small signal model.

III. THE PRINCIPLE OF ACTIVE INDUCTOR

Various versions of the simplest active inductor and the small-signal model are shown Fig.1. From the small-signal analysis, the nodal and loop equations can be expressed as

$$s \cdot C_{gs}V_{gs} + g_m V_{gs} = -I_x \qquad (1)$$

$$s \cdot C_{gs} V_{gs} R_g + V_{gs} = -V_x \qquad (2)$$

The equivalent impedance is

$$Z_{DS} = \frac{V_x}{I_x} = \frac{1 + s \cdot C_{gs} R_g}{g_m + s \cdot G_{gs}} \qquad (3)$$

$$Z_{DS} = s \cdot \frac{1}{\omega_T} \cdot \frac{R_g - g_m^{-1}}{1 + (\frac{\omega}{\omega_T})^2} + \frac{g_m^{-1} + R_g(\frac{\omega}{\omega_T})^2}{1 + (\frac{\omega}{\omega_T})^2} \qquad (4)$$

$$Z_{DS} = s \cdot L_{eff} + R_{eff} \qquad (5)$$

Thus the equivalent inductance is

$$L_{eff} = \frac{1}{\omega_T} \cdot \frac{R_g - g_m^{-1}}{1 + (\frac{\omega}{\omega_T})^2} \qquad (6)$$

And the equivalent resistance is

$$R_{eff} = \frac{g_m^{-1} + R_g(\frac{\omega}{\omega_T})^2}{1 + (\frac{\omega}{\omega_T})^2} \qquad (7)$$

So the effective quality factor can be written as

$$Q_{eff} = \omega \cdot \frac{L_{eff}}{R_{eff}} = \frac{\omega}{\omega_T} \cdot \frac{R_g - g_m^{-1}}{g_m^{-1} + R_g(\frac{\omega}{\omega_T})^2} \qquad (8)$$

At low frequencies, the active inductor has an impedance of about g_m^{-1}. At high frequencies, the low-pass filter formed by R_g and C_{gs}, cuts the gate-drain connection, causing the impedance of the circuit to increase similar to that of an inductor. It turns out that for $R_g > g_m^{-1}$, the impedance becomes inductive in a certain frequency range.

Fortunately, this inductance can be conveniently trimmed with the gate resistor R_g, while keeping the series resistance g_m^{-1} approximately constant for operating frequency much lower than the transit frequency (f_T). The active inductor can be used for frequencies up to about $f_T/2$. Compared with spiral inductors, active inductors are much smaller and more amenable to monolithic integration. For a common source amplifier (CSA) with active inductor loads, its voltage gain is about

$$A_v = \frac{g_{m_{MA}}}{g_{m_{ML}}} = \frac{\sqrt{\frac{W_{Amp}}{L_{Amp}}}}{\sqrt{\frac{W_{Load}}{L_{Load}}}}, (L_{Amp} = L_{Load} = L_{min}) \qquad (9)$$

It means that the voltage gain of this gain stage just depends on the aspect ratio between the input transistors and the load transistors and offers excellent immunity against the variations of process and temperature.

To verify the derived equations, Spice simulations based on $0.18\mu m$ CMOS are carried out and the simulated AC response are illustrated in Fig.2. From Fig.2(a), with the gate resistor increasing, the undesired peak goes higher corresponding to the increasing effective inductance, which confirms that this type of active inductor can be trimmed conveniently. Moreover, in the case shown in Fig.2(a), the optimal value of the gate resistor should be around 2KΩ, which is not a problem to implement such a resistor in modern CMOS technologies. Based on Fig.2(b), an active inductor with gate resistor has stronger shunt peaking effect than spiral inductor, while its low frequency gain is much lower when the gate resistor too large (band pass). According to the simulated data, higher
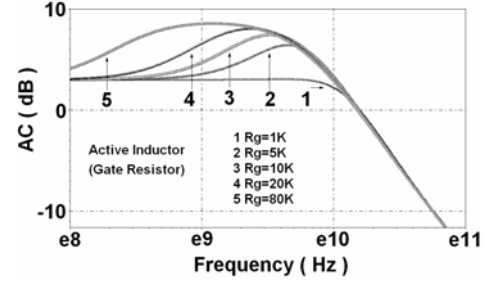
(a)
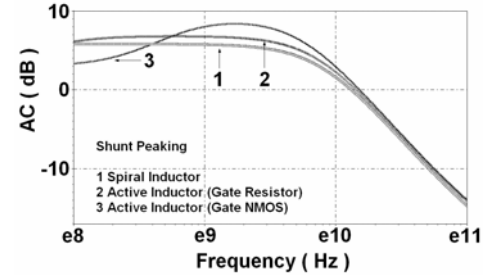
(b)

Fig. 2. AC response of shunt-peaked CSA: (a) Trimmable active inductor with a gate resistor R_g; (b) Comparison of shunt peaking inductors.

effective inductance can be achieved by using an active inductor with a gate resistor, which is not limited by finite self-resonance frequency, while on-chip spiral inductors with large inductance often suffer from low self-resonance frequency due to undesired parasitic.
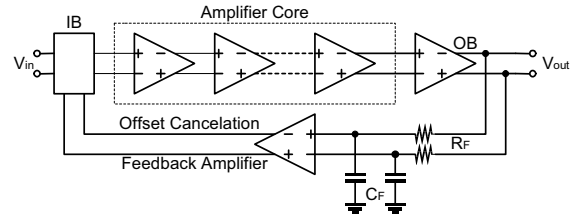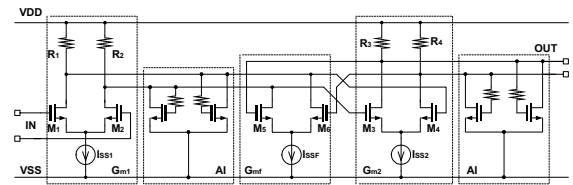

Fig. 3. Limiting amplifier architecture.

Fig. 4. Active feedback gain cell with modified active inductors for low supply LA.

IV. CIRCUIT DESIGN

A. LA Architecture

Shown in Fig.3, the proposed LA consists of a broadband input-matching network, three identical gain stages comprising the 10-Gb/s LA core shown in Fig.4, an offset cancelation feedback loop shown in Fig.6, and an output
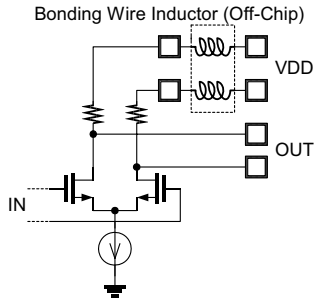
Fig. 5.   Schematic of the used output buffer.

Fig. 7.   Schematic of the used on-chip signal loss detection and alarm circuit.

buffer shown in Fig.5. The LA core must provide sufficient gain and bandwidth. It is, therefore, desirable to employ various bandwidth boosting techniques without introducing too much noise. Designed to operate as a standalone module, the LA must deliver large voltage swings to 50Ω loads, requiring a high-current output buffer. The core itself must provide a relatively large driving capability for the large input capacitance of the buffer.

B. Amplifier Core

A cascade of identical gain cells is used as the amplifier core to achieve enough voltage gain and -3dB bandwidth. However, a critical difficulty stems from the relationship between the number of gain cells, m, and the overall input-referred noise. For a larger m, the lower gain per stage leads to rapid accumulation of noise. For the input-referred noise levels targeted in this design, m must fall below approximately 6.

As shown in Fig.4, this work introduces active negative feedback as a means of improving the gain-bandwidth product (GBW) of amplifiers. Based on the discussion in [2], active feedback increases the GBW beyond the technology f_T by a factor equal to the ratio of f_T and the cell bandwidth.

In addition to active feedback, the proposed limiting amplifier employs the modified active inductor shown in Fig.4, which does not suffer from the limited voltage headroom while conventional active inductor does [5].
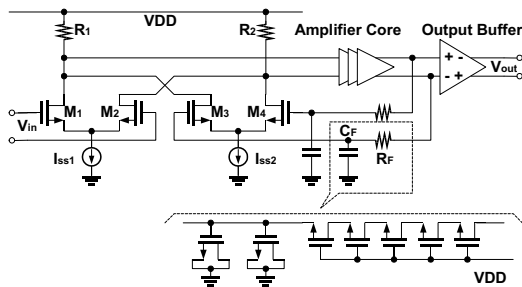

Fig. 6.   The used offset cancellation feedback circuit.

C. Output Buffer

Buffers driving off-chip loads typically present a bandwidth bottleneck resulting from the large input transistors that are necessary for high current drive capability. In broadband applications, the buffer must drive an on-chip
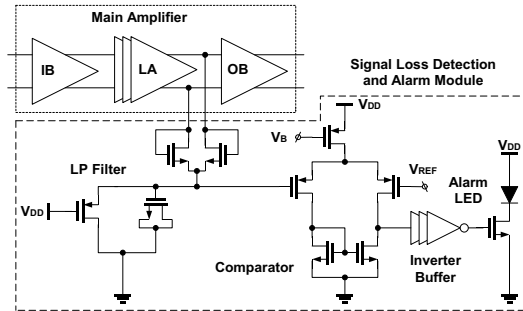
back termination resistor of about 50Ω in addition to an off-chip load of 50Ω. To deliver a single-ended voltage swing of 150mV to the equivalent resistance of 25Ω, the buffer must steer 6 mA, requiring a tail current of 8 to 10 mA when the incomplete switching of the stage is taken into account. Consequently, the input devices must be wide and bonding wire inductors can be used to partly tune out the relatively large output capacitance.

D. Offset Cancelation

The principal difficulty in the design of the offset cancelation loop relates to the required corner frequency f_c of the resulting high-pass filter. In order to ensure negligible droop in the output in the presence of long runs, f_c must fall in the range of a few tens of kilohertz. As shown in Fig.6, $R_F \cdot C_F$ must reach a few milliseconds for to be equal to a few tens of kilohertz. In this design, a 50MΩ active resistor serves as R_F and a 40-pF MOS capacitor as C_F, which are used to realize large value resistors and capacitors without chip area penalty.

Another issue stems from the low load resistance seen by the feedback amplifier at the input of the LA. To compensate for an input-referred offset voltage of roughly 20mV, and the differential pair of input stage must steer about 1mA to their loads while sensing an output offset of less than 10mV, a value determined by pulse width distortion requirements. Thus, these transistors must be sufficiently wide.

E. Signal Loss Detection and Alarm Module

To obtain signal loss information of the incoming data stream, an on-chip simple loss detection circuit is included as shown in Fig.7. Firstly the amplified signal was low-pass (LP) filtered by the proposed active low-pass filter and then the filtered signal was send to the input of the used voltage comparator and compared with the reference voltage. The output of voltage comparator is converted to rail-to-rail digital signal by cascading inverters to be used as the switching signal for the alarm LED (light emitting diode). Generally, there is no signal loss, LP filter outputs a higher voltage level than the reference and the output of the comparator is low. If signal loss occurs, the output signal level of LP filter will be lower than the reference voltage and the comparator will generate a "high" voltage level to turn on the alarm LED.
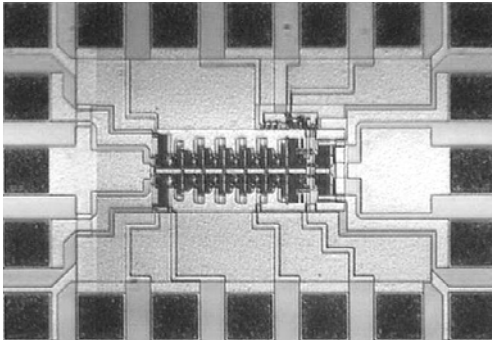
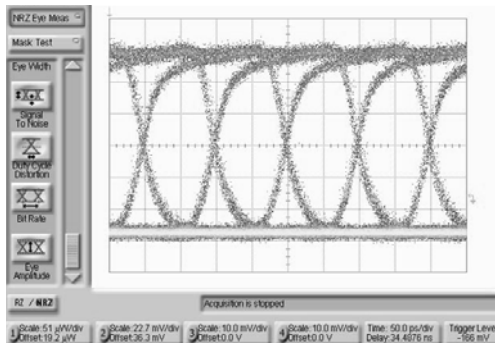Fig. 8.   Microphotograph of the implemented limiting amplifier.

Fig. 9.   10-Gb/s output voltage eye-diagram at $5mV_{pp}$ input.

V. Circuit Implementation and Evaluation

A. Circuit Implementation

The proposed 10-Gb/s LA was fabricated using 0.18μm CMOS technology. The microphotograph of the die is shown in Fig.8. The chip dimension including bonding pads are 1mm×0.7mm. The dimension of bonding pads is 0.1mm×0.1mm.

B. Circuit Evaluation

The performance of the fabricated chip has been evaluated via on-wafer probing on uncut wafers employing CASCADE MICROTECH probe station, an AD-VANTEST D3186 Pulse Pattern Generator, an ADVANTEST R6142 Programmable DC Voltage/Current Generator, a ROHDE & SCHWARZ SMP04 Signal Generator (10MHz-40GHz), an Agilent Infinium DCA 86100A Wide-bandwidth Oscilloscope and a HP 8593A spectrum
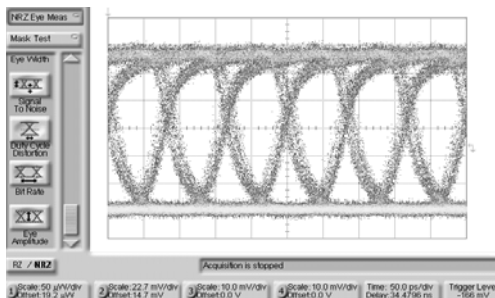

Fig. 10.   12-Gb/s output voltage eye-diagram at $5mV_{pp}$ input.

TABLE I
MEASUREMENT SUMMARY

Power	60mW
Supply	1.8V
Output Swing	125mV
Input Swing	4-400mV
Gain	46dB
Bitrate	10Gb/s
RMS Jitter	2ps

analyzer. Time domain characteristic was carried out by using differential $2^{31} - 1$ NRZ PRBS data streams generated by the pulse pattern generator.

As shown in Fig.9, the LA outputs a 10Gb/s voltage signal with a single-ended amplitude of $125mV_{pp}$ rather than the expected $150mV_{pp}$ due to the process tolerance of the used poly-silicon resistors (about 30% offset). Even though the signal swing observed from the oscilloscope is not high because of using small tail current of the output driver (just for the purpose of measurements), the internal signal level should be as large as the designed value to drive the following circuits (i.e. CDR).The RMS jitter is about 2ps and the minimum input amplitude is down to 4mV. This LA can operate up to 12-Gb/s illustrated in Fig.10 due to the use of effective bandwidth boosting techniques. This LA totally consumes 60mW which is the sum of 45mW dissipated by the core and 15mW consumed by the output buffer. The measurement results of the realized LA are summarized in Table I.

On the basis of above measured data, we can say that the proposed and realized circuits with active inductors can reach the same performance as its counterparts implemented with spiral inductors. However, the power dissipation is much lower and the chip size is smaller, which means they are better for low cost applications.

VI. Conclusion

A low power monolithic LA for low cost OC-192 optical communication systems has been implemented in 0.18μm CMOS. It turned out that on-chip active inductors combined with other bandwidth boosting topologies can eliminate the trade-off between gain-bandwidth product and power consumption. Based on the observed performances of the implemented chip, it is very promising to develop low power compact CMOS circuits using active inductors rather than area-consuming spiral inductors for 10-Gb/s optical networks.

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