DS/Chirp Hybrid Industrial UWB System for Ranging and High Reliability Communications

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Abstract— **In this paper, we propose chirp UWB system applied to industrial application. Reliability is highest demand for industrial applications, therefore, same high reliability and stability performance are also required in wireless communication systems for such applications. Since chirp scheme can be exploited stable communication performance under harsh multi-path communication environment, excellent performance is expected in the industrial scene where it is severe communication environment often we encounter. However, in an employment of chirp scheme, symbol timing detection is often problem in receiver end. Therefore, in the proposed system, DS spread spectrum modulation is applied to its preamble. This enables establishing carrier synchronization without performing any carrier synchronization procedure. Furthermore, in an employment of the proposed scheme, it enables very precise ranging and channel estimation function. This paper presents system configuration of the proposed scheme and evaluation results of its characteristics by computer simulations.**

Index Terms— **chirp signal, DS, industrial wireless communication, ranging, preamble, UWB**

I. INTRODUCTION

Radio system for industrial applications, such as manufacturing control data communication, machine tool control communication, and industrial mobile communications; for example Automated Guided Vehicle (AGV) used in a semiconductor factory and a LCD factory, a warehouse cart and a picking cart.

Since industrial mobile systems are continuously moving in a factory and communicate each other, therefore identification of its location is very important to perform effective control and system management. And this identification and communication leads to improvements both dispatching efficiency and operation stability. Wireless systems that have been used in such industrial application are: a very weak radio, a low power radio, wireless LAN and ZigBee [1], and these are already used in such areas. However, many of these do not have a ranging function. Therefore these systems cannot apply to the ranging applications to obtain location information.

Also if we realize the ranging function with the conventional systems, there are existing systems which utilize the Received Signal Strength Indicator (RSSI) to measure the distance. But since the system only use received signal power, it cannot realize very high and precise ranging performance.

On the other hand, UWB is now highlighted to be able to realize very high-speed communications. And also, not only high-speed communications but also ranging function can be performed [2]. Furthermore, very precise ranging performance is expected. The formerly introduced schemes of UWB are DS-UWB and MB-OFDM, and other many ways are also now in considerations.

We applied chirp UWB as our proposed system. The chirp schemes can be realized with relatively simple circuit, and can generate UWB signals. There is flexibility to adopt specified (radio-regulation) spectrum mask and also the chirp scheme has characteristics of reliability and robustness in multi-path fading channel for the industrial application environment where very high relatively is required.

In such industrial hash communication environment, the very robust system required. So the chirp scheme seems the optimal solution for such applications. However if employ the chirp schemes, receiver timing detections problem arise. From this reason, we propose employment of Direct Sequence Spread Spectrum (DSSS) modulation to the preamble and it is enabled to establish timing synchronization without performing any carrier synchronization. Employment of this scheme also makes it possible to exploit high precision ranging and channel profile estimation function.

In this paper, we explain the proposed DS/Chirp hybrid UWB system's configuration, which enables high reliability communication and ranging for industrial application wireless systems. And we evaluated its characteristics, especially sampling clocks relationship and ranging function by computer simulations.

II. DS/CHIRP HYBRID UWB SYSTEMS

At the beginning, we explain about the proposed system's configurations. On a transmitter end, this block is configured by a preamble transmission block and a chirp wave generation/transmission block. On the receiver end, an IQ conversion block, a DSSS demodulation block and an Analog to Digital Conversion (ADC) block are configured. Fig. 1 and Fig. 2 show configurations both transmitter block and receiver block respectively.

A. Chirp UWB

The proposed scheme employs the chirp scheme for data modulation. The chirp scheme is expected its very high performance by its characteristics for industrial wireless communication applications. 4-ary chirp transmission chirp signal *s(t)* is explained as

$$s(t)=\begin{cases} A\sin\left[2\pi\{f_0+M(k)f_d\}t+D(k)\frac{1}{2}\mu t^2\right] & |(t-nT)<<T| \\ 0 & otherwise \end{cases} \tag{1}$$

where A is envelope level of transmitter signal, f_0 is center frequency, μ is sweeping center frequency, T is repetition interval, *M(k)* is frequency shift direction if *k*th symbol (+/-1), and *D(k)* is *k*th transmission information (+/-1).

There are many ways to generate chirp signal. The proposed system uses very wideband Voltage Controlled Oscillator (VCO) to generate the chirp signal. By employing the VCO, the chirp signal can be easily obtained without using any expensive devices (e.g. saw device). Also implementation of voltage tuning control for VCO enables generation of chirp signals at any frequencies. So it is possible to generate the signal very flexibly. The chirp signal for the data modulation, each bit is mapped into up-chirp and down-chirp. And further, occupied bandwidth of 500MHz is divided into two sub-bands, these make four states as one symbol. Then it enables to transmit two bits per symbols as the 4-ary chirp scheme.

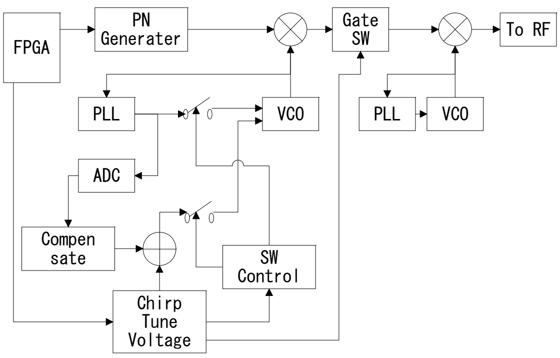

Fig. 1 Transmitter Block

Employment of the chirp schemes can be obtained flowing merits. Relatively simple circuit enables generations of wide range UWB signal. Consideration of very wide band group delay characteristics can be absorbed. It is very robust for multipath delay spread.

However, in an implementation of actual circuitry, the following points become problems. If the chirp scheme is employed to realize our proposed system, it is difficult to detect symbol timing of the chirp symbol on the receiver end. To achieve very high precision and resolution, very precise time and pulse location measurement are required. To solve above problems, the proposed system employs DSSS modulation to the preamble.

B. DSSS modulated preambles

On the signal reception, if the receiver does not perform any carrier synchronization to the received signal, the frequency offset statically exists between transmission and reception end. On the chirp signals reception, this offset would affect performance. Also precise symbol point detection becomes much difficult. Therefore, we employed DSSS modulation to the preamble. This is to establish synchronization without performing any carrier synchronization. The preamble signals *s(t)* is explained as

$$s(t)=A\sum_{j=-\infty}^{\infty}c(m)d^{\alpha/\beta}(n) \tag{2}$$

$m = j \bmod M$, $n = \lfloor j/M \rfloor \bmod N$

where c is inner code and $d^{\alpha/\beta}$ is outer code and,

$$d^{\alpha/\beta}=\begin{cases} codeword \quad \alpha \quad data=+1 \\ codeword \quad \beta \quad data=-1. \end{cases}$$

On the receiver end, received signal is split into I and Q phases. Each signal is then de-spread with inner spreading code sequence and actual correlation output is obtained by vector signal composition of the I and Q output. If the inner code length is small, it is possible to spread without concerning any carrier slip between the transmitter and the receiver. If we accept less than 45 degrees IQ rotation as a limit, we can assign total code length of 2000 chips where the range without considering carrier phase shift. From this limitation, we assign enough short 11chip length to the inner code (barker sequence).

For the ranging, time interval measurement is performed by measuring the position of peak output of the code. This position is determined by time counting of the inner code peak output timing by time interval measurement block operation. However, only employment of the inner code, the maximum ranging distance becomes short because of ranging limitation of the inner code length. To solving this, concatenated outer code is employed. This concatenated outer code performs coarse location decision and expansion of the ranging distance. Also this concatenated code is used for the frame synchronization.

By applying the DSSS modulation to the preamble, it enables both synchronization and ranging without performing any carrier synchronization. Furthermore by exploiting the synchronization timing by the preamble, it enables phase compensation of the chirp signal (payload field) receiving.

In the transmitter, during the preamble is transmitted, the VCO is controlled by Phased Locked Loop (PLL) and transmission is performed. When the chirp signal payload field begins, PLL becomes absence and the chirp signal transmission is performed by being applied to VCO voltage control signal from saw waveform generation circuit. In the chirp transmission time, the VCO becomes free-run conditions then the frequency shift of VCO is appeared. Therefore the VCO controlled voltage must be compensated with DC level, which precise level sampled during the preamble transmission (PLL controlled) timing. And then the saw wave VCO controlled voltage is offset and compensated during chirp signal transmission. As explained, by employing DS/Chirp hybrid schemes, we can overcome many problems realizing the chirp UWB system.

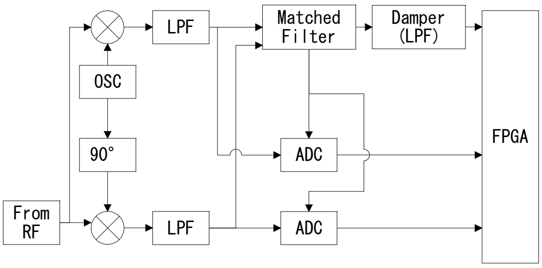

Fig. 2 Receiver Block

C. Concatenated Code

Concatenated DS code is used. For the inner code, length of 11 chip barker sequences is used for the bit synchronization. The outer code is length of 31 chip Gold sequence for the frame synchronization. If we assume 4 bits for synchronization code, total preamble length of 1364 chip is obtained.

Furthermore, preparing several number of different outer code sequences, it is possible to separate its network into pico nets each other. For example, if we prepare 4 kinds of codes, 255 pico nets can be controlled.

D. Receiver block

Both the bit synchronization and the frame synchronization operation are performed at the DSSS receiving block. At first, at the inner code despreading, we obtain correlation output. On the outer code despreading, keen correlation peak output signal, which obtained by inner code despreading is transformed into lower rate by damper circuit and then outer code despreading is performed by digital processing. The outer code sequence is decoded with predefined sequence to establish frame synchronization.

The received chirp signal is IQ converted then fed to ADC block. The ADC block performs symbol phase shift compensation. Because the chirp signal is completely works in asynchronously, symbol point phase offset will be appearing. Therefore signal is oversampled at the before/after of the symbol point. And these sequential data (which assumes its symbol point is its center data) are temporally stored into the memory in the ADC block. To these stored data, its symbol phase offset is compensated by the synchronization timing signal generated by DSSS preamble. The compensated data is fed to the matched filter and the signal is extracted by maximum likelihood operation.

E. MAC Protocol

In the proposed scheme, it is possible to perform the ranging by the preamble. Therefore both communication and ranging can be simultaneously performed in the system. From this reason, unique MAC protocol is designed. This MAC protocol is changed by the packet structure of IEEE802.15.4. On the other hand, to obtain higher level of ranging performance, we prepared another packet length outer code for the option. Its details are explained in 3-3. So far we explained are the hardware and MAC configuration of the proposed system.

III. Ranging Algorithm

In here, we explain about the ranging schemes of the proposed system. In the measurement of ranging in conventional wireless systems, Arrival of Angle (AoA; which estimate the location by direction of the signals), Received Signal Strength Indicator (RSSI; calculated the length by received the signal strength) and Time of Arrival (ToA; performed by measuring the timing) exist. To realize ranging function in the proposal system, we employ Double Token Exchange ToA (DToA) scheme.

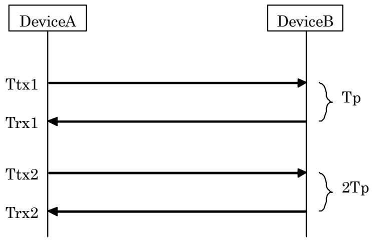

Fig. 3 DToA scheme

A. DToA Ranging Scheme by Employing DSSS

In this system, the timing measurement performed by preamble. This enables precise and accurate measurement. From this, false detection probability of pulse location can be minimized in the DTOA scheme. In Fig. 3, measurement sequence of proposed DTOA scheme is illustrated.

$$t_l = (t_{rx1} - t_{rx1}) - \{(t_{rx2} - t_{rx2})/2\} \quad (3)$$

where t_l is propagation time, t_{tx1} And t_{tx2} are transmission invoking times, t_{rx1} And t_{rx2} are receive complete times.

$$d_l = ct_l \quad (4)$$

where d_l is Measurement distance, and c is light speed

Transmit station (Device A) becomes control station, then the station controls all of the communication sequences

B. Measurement Algorism

Algorism of the measurement is performed as blow.

1) Transmit station (Device A) transmits the packet. The station saves the preamble transmission timing of t_{tx}.

2) Receive station (Device B) retransmits the returning packet with the internal processing timing t_p after receiving the packet

3) On the transmit station end, it receives the returning packet from the receive satiation. The receiving timing t_{rx} is stored. This timing t_{rx} is at the frame synchronization (at the packet preamble shown above) is succeed.

4) Sequences 1), 2) and 3) are repeated several times. In the sequel, the transmit station obtains propagation time. And distance is calculated by this obtained time value.

To eliminate the effect of the processing time, the obtained time value is compensated with the response delay timing, e.g.

outer code shift timing and other compensation parameter etc. Then distance estimation is performed. In the timing measurement block, the inner code correlation output location is continuously measured to identify the chip number location. Hence the time measurement can be performed. Additionally, exploiting the outer code chip timing, it enables long-range measurement by coarse positioning detection with the outer code sequence. At the timing measurement block, high-speed digital clock is prepared and this clock is used to perform measurement.

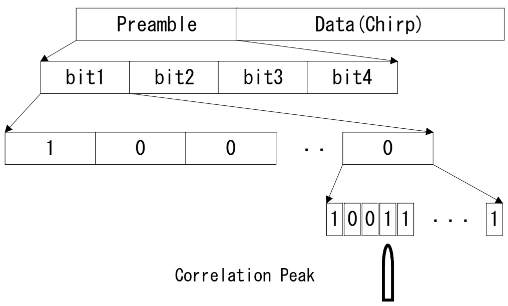

Fig. 4 DS Sequence for the Ranging Measurement

C. DS Sequence for the Ranging Measurement

As an another option to improve the ranging performance, we changed the outer code in the preamble. By employing longer code for the outer code sequence, extension of the ranging distance between two terminals is possible. Prior to performing ranging measurement sequence, each terminals exchange information regarding transmission packet format. This makes appropriate reception for each different packet format

IV. SYSTEM SIMULATION

For system simulation, if we consider about the use in industrial applications, the required performance is varies depend on applications. For example, if we assume AGV application, the communication data lengths of relatively short (several ten bytes) are expected. It is because the primary exchanging data are control data and sensor data. In the ranging operation, if the ranging measurement result is used to improve AGV's dispatching efficiency and to avoid AGV collision, the required ranging resolution varies depending on AGV's moving speed and number of AGV in the system.

In this simulation, our standard condition in industrial application is assumed. Transmission packet size is set to 31 bytes. Ranging error is defined less than 1 meter. We evaluate the performance of the proposed system by computer simulations.

In the proposal system, which the DSSS preamble is used, it is possible to realize the precise symbol detection. However by the realization of the real hardware, the limitation of the ADC and sampling clock speed of the digital processing becomes a problem. Hence the discussion in this paper, about the definition of maximum sampling clock rate, we must consider the devices that can be obtained in the real world. We evaluated chirp signal demodulation, how the phase offset compensation becomes close to the ideal positioning. Simulation specification is shown in Table 1.

TABLE I
SIMULATION SPECIFICATION

Modulation scheme	DS (preamble portion) 4-ary chirp (data portion)
Spreading bandwidth	500MHz
DS code	inner code barker sequence outer code Gold sequence
Chirp ADC # of sample	ADC sampling number of 4, 8 samples
Packet size	31Bytes
Channel	AWGN

A. Symbol Phase Compensation Characteristics Using DSSS Preamble

Symbol phase compensation characteristics of the preamble are evaluated using Bit Error Rate (BER) and Packet Error Rate (PER) characteristics in the view point of sampling digital clock speed. In here, we assume that no carrier synchronization between the transmitter and the receiver is performed. And also we assume that the state where the phase offset will arise during data reception.

In the BER characteristics, the reception of preamble is assumed to be perfect and we performed the simulation as the sequence that an establishment of both bit synchronization and frame synchronization are performing. The performance of the phase offset compensation is evaluated during chirp signal receiving. For the PER characteristics, we evaluated it in the condition where the preamble reception is included. Also the phase offset value is assumed to be known when preamble receiving is succeeded.
The symbol phase offset compensation, the sampling point of ADC is assumed to be 4 and 8 point. And the compensation is performed in this two sampling speed. For comparison, we confirmed in the condition where phase compensation is performed ideally. In Fig. 5 and Fig. 6 show BER and PER characteristics respectively, in the simulation, it is observed that the characteristic becomes good if the number of sampling point is increased. This lead to phase compensation value can be tuned much fine. If the number of sampling point is 8, performance degrades only 2dB by ideal state.

B. Ranging Performance

We also confirmed the ranging performance using the DSSS preamble. Because the ranging is performed at the preamble portion in the proposed system, total packet length can be shortened if we can shorten the preamble length. It leads to the possibility to increase the throughput etc.

On the other hands, it is also possible to extend the ranging range if we employ longer sequence length for the outer code in the concatenated code.

From these reasons, we confirmed average ranging error characteristics when outer code length of the concatenated code is changed. In the simulation, we assumed the code length of 15, 31 and 128. For each situation, the frame synchronization code is assumed to be 4bit. And also it is assumed that the ranging is properly performed if the frame synchronization is achieved. In Fig. 7, it is shown that average ranging error characteristics if the outer code of the concatenated code length is extended.

Improvement of the characteristics is observed when longer outer code length for the concatenated code is employed. This is because the frame synchronization succession rate is increased when the code length becomes longer. However, ranging resolution is determined by the inner code, improvement effect becomes smaller if the code length gets longer. Also it is possible to extend ranging range, if the outer code property is changed. But the communication distance performance itself is limited because of limitation of transmission power regulation. We took into account this problem and determined to select the code length 31 in the usual situation and code length 127 when the ranging resolution is primary importance.

V. CONCLUSION

In this paper, we proposed DS/Chirp hybrid UWB system for UWB wireless system for industrial applications. And also in we performed computer simulation, we confirmed fine characteristic of the proposed scheme. Especially in the simulation, we focused the rate of sampling digital clock of the proposed scheme. By employing DS/Chirp hybrid scheme using DSSS modulation at the preamble, we confirmed that very high performance is obtained with overcoming the actual circuit realization problem. The DSSS preamble compensates the phase offset of the symbols, it makes optimally receiving conditions. We confirmed that very good performance is achieved in UWB systems. And also the upper bound of the sampling clock limitation is confirmed. Additionally in ranging with the DSSS preamble, we also confirmed that detection error goes lower in the harsh industrial environment.

In further study, we will implement the proposed schemes to the actual evaluation system and performance evaluation will be also performed with the actual systems.

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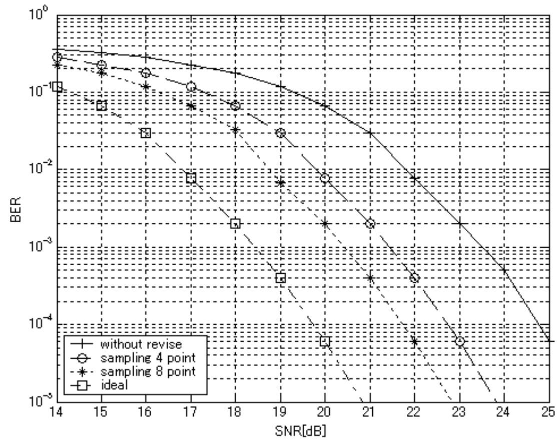

Fig. 5 BER Performance

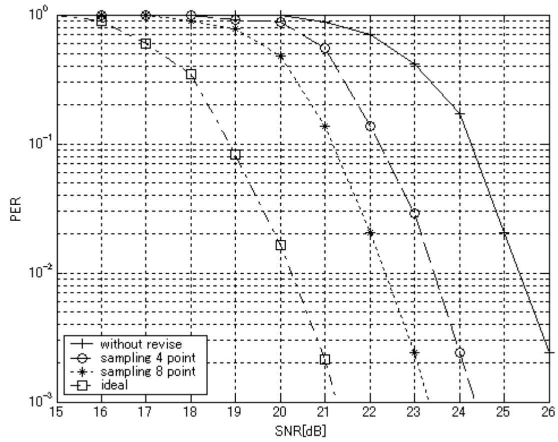

Fig. 6 PER Performance

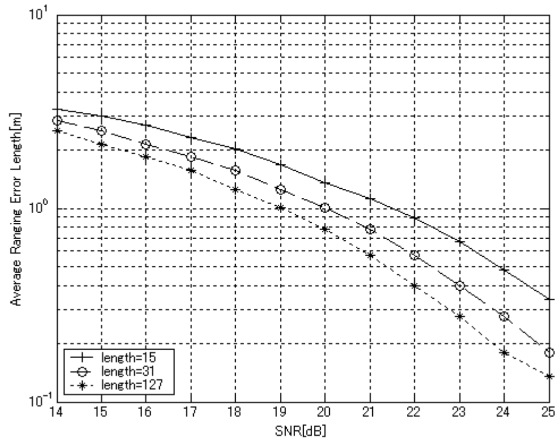

Fig. 7 Ranging Performance