Designing Test Patterns for Effective Measurement of Typical TSV Pairs in a Silicon Interposer

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Abstract— **In this paper, practical test patterns are designed to calculate the characteristics of Through-Silicon Via (TSV) pairs in a silicon interposer. Proposed test patterns include probing pads, traces and TSVs, which are modeled by a combination of impedances and admittances. Performance of the test patterns is obtained from simulation models built in full wave simulation solver. TSV response is then obtained by de-embedding the pad and trace from the test patterns. The TSV response is also verified by analytical TSV characterization and full wave simulation results for only TSV structures. Thus the paper provides a guide to design feasible test structures from which true response of a TSV pair can be derived.**

Keywords—TSV; de-embedding; analytical; full wave simulation

I. Introduction

Currently, scaling in feature size has moved forward to deep submicron nodes according to Moore's Law. However, traditional two-dimensional system-in-package (2D SiP) can no longer support the scaling of size, power, bandwidth, and cost at the same rate. To meet these challenges, three-dimensional integrated circuits (3D-ICs) are implemented. 3-D ICs have many advantages such as more functionality, higher performance, better noise immunity, reduced power consumption, and faster speeds. In 3-D ICs, chips are stacked vertically in a small space, increasing the integration density while keeping the same packaging size. 3D ICs offer a more efficient way to allow different types of electronic, optical and electro-mechanical components to be integrated into a single package. Through-silicon-via (TSV) is the core technology in 3D ICs, used to connect two active layers in the vertical direction. The TSV is a very promising technology that enables short electrical delay, high interconnection density, small form-factors and low power consumption [1].

As the TSVs play an important role in the design of 3D ICs, it is essential to characterize the electrical properties of the TSVs in order to better analyze the 3D ICs' performance. The IC structures can be characterized by vector network analyzer measurements using micro-probes. However, due to the fabrication process, the TSVs are not directly accessible, and if access to TSV is made possible somehow then TSV diameter is too small to directly and reliably land micro-probes. So probing pads are provided on topmost metal layer and are connected to the TSVs by traces on the closest metal layer. This enables access to TSVs for network parameter measurements. Well-designed test patterns for pads, traces and TSVs are required to extract the characteristics of TSVs independent of the test fixtures [2, 3]. In [2] an extended L-2L de-embedding method is proposed to investigate the RF characteristics of TSV. This method works for small resistance and inductance of TSV but is very sensitive to the variation in the length of the transmission line, which is unavoidable in the manufacturing process. In [3], electrical model of TSV is extracted using silicon photoconductive properties up to 20 GHz. But this method requires the full structure under test to be symmetric and a beam of light is required to apply on the circuit to modify the conductivity of the substrate, which increases the complexity of the measurement.

In this paper, simple test patterns for the effective measurement of typical TSV pairs in silicon interposer are presented. Section II covers the core methodology to use five different test patterns to extract the electrical characteristics of a TSV pair. The TSV pair is modeled as a T-network and individual components of this model are computed. Section III will briefly introduce the analytical method for TSV characterization borrowed from [4] which is based on resistance–inductance–capacitance–conductance (RLCG) model for TSVs. The solution is used to obtain comparable T-network components. The de-embedding methodology and analytical formulation are then used to get network parameters for a practical geometry as described in Section IV. The results are compared to real TSV performance from full wave simulations. Section V concludes the work with some discussion about the practical application of the work and the difficulties in the method presented.

II. Methodology

The proposed de-embedding method to remove the effect of pads and traces is illustrated in this section. Fig. 1 shows the geometry for the first three test patterns and their models. These patterns have the pads and traces with no TSV connected to them. First two patterns, 'Open' and 'Short', are simple the pads and traces with open and short load condition. 'Short' uses a trace of same length as the TSV pitch to short the two traces of the pattern. The third pattern 'Short2' uses a trace of twice the length as 'Short' to connect the traces from each pad.

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The patterns are used to characterize the pads and traces as lumped elements Y_x and Z_x, representing the shunt admittances and series impedances of the contact pads and traces. Z_{line} represents the impedance of the extra trace used in the 'Short' pattern. In 'Open' pattern, Y_x is equal to Y_{Open}, which is the admittance looking into the 'Open' pattern as shown by

$$Y_x = Y_{Open} . \quad (1)$$

Similarly the Y_{Short} and Y_{Short2} are the admittances looking into the port for 'Short' and 'Short2' patterns, as shown in (2) and (3), respectively. 'Short' and 'Short2' use traces with different lengths to implement the short path. Assuming Z_{line} is proportional to the length of the trace, from (2) and (3), Z_{line} can be found as shown in (4)

$$Y_{Short} = Y_x + 1/(Z_x + Z_{line}) , \quad (2)$$

$$Y_{Short2} = Y_x + 1/(Z_x + 2Z_{line}) , \quad (3)$$

$$Z_{line} = 1/(Y_{Short2} - Y_x) - 1/(Y_{Short} - Y_x) . \quad (4)$$

From (2), Z_x can be found using (5)

$$Z_x = 1/(Y_{Short} - Y_x) - Z_{line} . \quad (5)$$

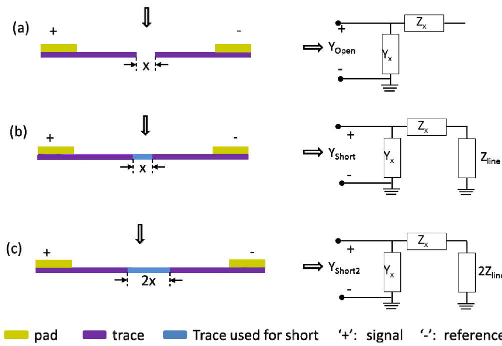

Fig. 1. Geometry of three test patterns and corresponding models for the pads and traces with no TSV connected in (a) open and (b),(c) short load condition.

Fig. 2 shows the remaining two test patterns, which consist of the pads, traces, and the TSV pair. The two patterns have different load conditions, namely open or short. The model for the TSV pair is a symmetrical T-network to represent the series and shunt impedances, Z_1 and Z_2, respectively. For the open condition, the load is assumed as ideal open, but for the short condition, the impedance of the short is represented by Z_{Short}, which will be non-zero for a practical implementation. Independent of the load condition, the effect of pad and trace can be removed using (6), where the $Y_{Original}$ and $Z_{De\text{-}embedded}$ are the Y and Z parameters before and after removing the contribution of pads and traces (Y_x and Z_x), respectively.

$$Z_{De-embedded} = 1/(Y_{Original} - Y_x) - Z_x . \quad (6)$$

Using (6) for each case, the impedance looking into the TSV pair after de-embedding can be written as

$$Z_{TSVopen} = 1/(Y_{TSVopen} - Y_x) - Z_x , \quad (7)$$

$$Z_{TSVopen} = 1/(Y_{TSVshort} - Y_x) - Z_x . \quad (8)$$

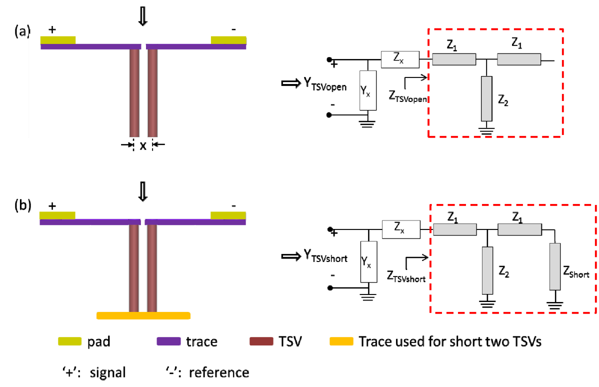

Fig. 2. De-embedding model for $Z_{TSVopen}$ and $Z_{TSVshort}$ extraction.

The resulting models of the two test structures with TSV after de-embedding are marked with the dashed red rectangles in Fig. 2. The input impedance of the two models can be used to solve for Z_1 and Z_2, provided the Z_{Short} (impedance of structure used to implement a short on the bottom side of the interposer) is known.

$$Z_{TSVopen} = Z_1 + Z_2 , \quad (9)$$

$$Z_{TSVshort} = Z_1 + (Z_1 + Z_{Short}) // Z_2 . \quad (10)$$

Solving for Z_1 and Z_2 from (9) and (10)

$$Z_1 = Z_{TSVopen} + Z_{Short} - \sqrt{(Z_{TSVopen} + Z_{Short})^2 - (Z_{TSVopen} Z_{TSVshort} + Z_{Short}(Z_{TSVshort} - Z_{TSVopen}))} , \quad (11)$$

$$Z_2 = Z_{TSVopen} - Z_1 . \quad (12)$$

The choice of Z_{Short} influences the value of Z_1 and hence the value of Z_2. For an implementation with very low value of Z_{Short} compared to Z_1 and Z_2, Z_{Short} chosen as zero will have little influence on the results. However, if Z_{Short} is comparable to the value of Z_1, then the value has to be carefully estimated as it will significantly influence the value Z_1. In this paper, for the Z_1 and Z_2 calculation, Z_{Short} is considered as a perfect short (zero). In the real implementations, depending on the fabrication capability, the short on the bottom of interposer could be a large solder bump, or a trace, whose impedance will be no-zero.

Using this de-embedding method, impedance of the TSV pair can be extracted conveniently. The choice of Z_{Short} controls the accuracy of the Z_1. Better results can be obtained based on information about the implementation of the short standard. An application of this methodology is shown in the Section IV.

III. Analytical Method

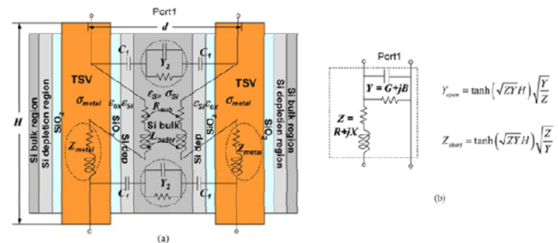

Fig. 3. (a) Equivalent distributed circuit model of a single pair of TSVs and (b) the distributed transmission line model [4].

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In [4, 5], an equivalent distributed circuit (RLCG) model is proposed for a pair of TSVs. The MOS effect and AC conduction in silicon, the skin effect in the TSV metal, and the eddy currents in silicon are considered for the high-frequency analysis in this model, as shown in Fig. 3.

This modeling method is used to calculate the analytical impedance parameters of a single TSV pair to verify the feasibility and accuracy of the proposed de-embedding method. For a one-to-one comparison between the analytical model and the proposed TSV model, the Z_1 and Z_2 are calculated using the relationship given by

$$Z_1 = \frac{Z}{2}, \quad Z_2 = \frac{1}{Y} \tag{13}$$

where Z and Y are the per unit length series impedance and the per unit length admittance for a single TSV pair in [4,5].

IV. APLLICATION

In this section, the five test patterns, introduced in Section II, are built and simulated in a full wave solver to demonstrate the proposed de-embedding method. The results of the de-embedding method are compared to the results from the analytical method from Section III and the results from the simulations of only TSV structures. The first three test patterns provide the model elements corresponding to the pads and traces. These are used with the results of the last two patterns, which include TSVs to remove the effect of pads and traces. Then these results are used to further derive the elements of the TSV pair's T-network model.

All the models consist of three generic parts: pads used for landing micro-probes, traces used to connect the TSVs to the pads, and the TSV pair to be studied. The pads are 40 µm ×40 µm squares, and 200 µm apart, and start from metal layer of the trace and go to the top layer where they are accessible to the probes. The traces are 1 µm thick and 10 µm wide, on the first metal layer form the silicon, connecting the TSVs to the pads. The TSVs are 10 µm in diameter and placed with a 20 µm pitch. A dielectric layer SiO_2 (with thickness of 0.5 µm) surrounds each TSV to isolate them from the Si interposer. Fig 4 shows the pads, traces, and TSV structure's top view and cross-section with their dimensions.

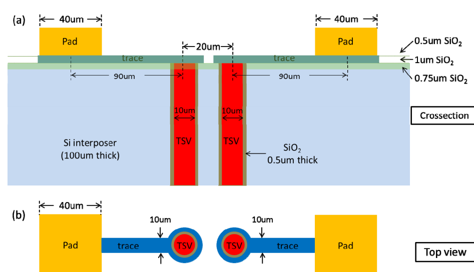

Fig.4. (a) Top view and (b) cross-section of pads, traces, and TSVs with dimensions.

Five models are generated in a full wave solver based on the proposed patterns as shown in Fig. 1 and Fig. 2. The shorting trace lengths in 'Short' and 'Short1' patterns are 20 µm and 40 µm respectively. Copper disc with diameter of 100 µm is used to short two TSVs. A lumped port is set between the two pads to excite the structure in a manner similar to a probe landing for real measurements. The frequency range for the simulations is from 50 MHz to 50 GHz.

To verify the accuracy and feasibility of the de-embedding patterns, two more models are created in HFSS, in which only TSV pair is set up, as shown in Fig. 5. The purpose of these only TSV pair models is to get the simulation results for a real TSV pair without the inter-connects, which can be compared with the calculation results of the de-embedding method in both open and short termination cases. Lumped port is used at the top of the two TSVs as the excitation source, and the TSV pair uses the same geometry as the test patterns. The models in Fig. 5(a) have real terminations (as would be implemented on a interposer), and the models in Fig. 5(b) have ideal terminations using PMC and PEC surface to get an ideal open and short without the parasitic termination impedances. The ideal TSV case is used to analyze the accuracy of the T-network model for TSV, to verify that it is independent of the fixture effect (non-ideal short/open effect).

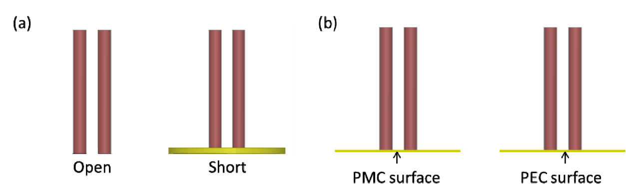

Fig.5. Models generated in a full wave solver for only TSV pair with (a) real terminations and (b) ideal terminations.

Y_x, Z_{line} and Z_x, calculated using (1), (4), and (5), are shown in Fig. 6. As discussed in Section II, two patterns are used with different length of short standard to calculate the impedance of the short, Z_{line}. It can be seen that, the Z_{line} is resistive at low frequency and becomes inductive as the frequency goes up.

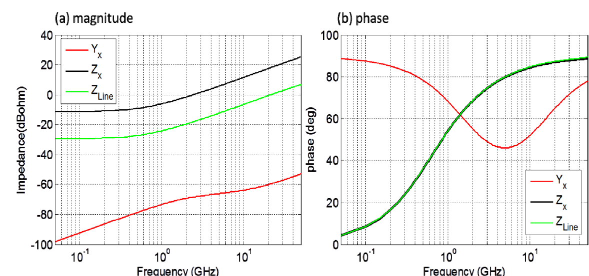

Fig. 6. (a) Magnitude and (b) phase of Y_x, Z_x and short impedance Z_{line}.

A. Z parameter results in TSV open case

Fig. 7 shows the comparison results for Z_{IN} in open case, calculated by use of de-embedding method (green), and extracted directly from full wave simulation models (red), respectively. The Z_{IN} of the TSV pair is capacitive at low frequency and then resistive around 2 GHz to 10 GHz, and then becomes capacitive at high frequency.

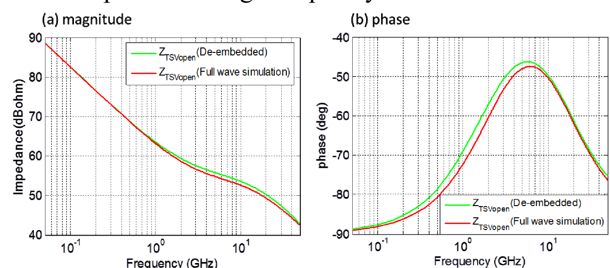

Fig. 7. Z_{IN} comparison when the TSV pair is in open case.

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B. Z parameter results in TSV short case

Fig. 8 shows the comparison results for Z_{IN} in short case. The green and red lines represent the Z_{IN} results calculated by de-embedding method and full wave simulation, respectively. It is shown that resistance dominates at low frequency while inductance dominates as the frequency goes up.

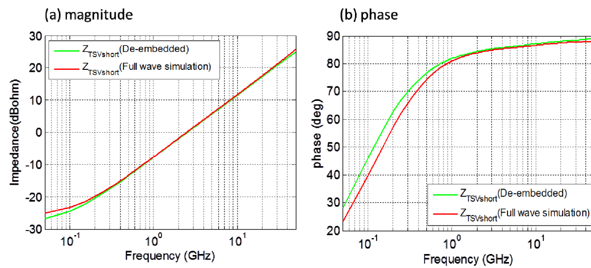

Fig. 8. Z_{IN} comparison when the TSV pair is in short case.

It can be seen that, the Z_{IN} obtained from de-embedding method and full wave simulation with only TSV pair have a good match for both open and short load conditions.

C. Z parameter for T-network model

To further analyze the accuracy of the proposed T-network model for TSV pair, Z_1 and Z_2 are calculated, using de-embedding results, analytical method and full wave simulation for a TSV pair with ideal open/short terminations.

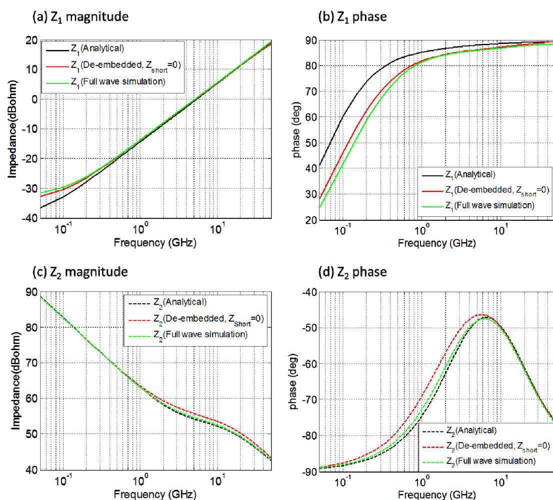

Fig. 9. Z_1 and Z_2 comparison of the de-embedding, analytical and full wave simulation method.

Analytical results are calculated based on Section III, as shown in black in Fig. 9. The comparison in Fig. 9 shows that our de-embedding model for a TSV pair agrees with the analytical model up to 50GHz. Full wave simulation results, shown in Fig. 9, for a TSV pair with ideal open/short terminations (model shown in Fig. 5(b)) are used with (11) and (12) to get a reference for comparing the equivalent TSV model.

V. OBSERVATION AND DISCUSSIONS

Five simple test patterns are proposed for the measurement of a TSV pair, using only one port. TSV pair is characterized with a symmetric T-network model, without two-sided probe-measurements, in which probe landing is far more difficult. In addition, the complexity of the manufacturing process is much larger to fabricate the pads and traces on the bottom side of TSV pair.

The open and short standards used in the test patterns to calculate the T-network elements are not ideal, due to the capacitance in the 'open' patterns and resistance and inductance in the 'short' patterns. For the short standard implementation, a large disc is used to short the TSV pair. The disc shape and size minimizes the parasitic effect of short, but is not zero as used for Z_{Short} in the calculations. This introduces the small inaccuracies in T-network model calculation.

It can be demonstrated that the error in the de-embedding process (removing effect of pads and traces) can propagate to the T-network model calculation for TSV pair. The comparison to TSV structures and analytical solution in Section IV-C shows that this error is small, and that such measurement using proposed test patterns is feasible to characterize TSV pair.

VI. CONCLUSION

In this paper, simple test patterns are proposed for effective de-embedding of test fixtures from the measurements of TSV pairs in a silicon interposer. The single port measurements for the proposed test fixtures are used to model the TSV pair as an equivalent symmetric T-network. This model has been verified with an analytical solution and full wave simulations, both independent of the test fixture.

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