Crosstalk Rudction in TSV Arrays with Direct Ohmic Contact between Metal and Silicon-substrate

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***Abstract*—In response to the requirement of novel crosstalk-reduction scheme for high density through silicon via(TSV) interconnects in silicon interposer, this paper presents a structure and performance analysis of through-silicon via(TSV) with direct ohmic contact between a ground TSV and silicon substrate for coupling mitigation purposes. We further expand the structure to a 3x3 TSV array and investigate its cross-talk performance. The simulation results show that the signaling scheme, which uses direct ohmic contact for ground TSVs, can effectively reduce the crosstalk and coupling noise between signal TSVs than the conventional design.**

Keywords—Cross-talk, direct ohmic contact ground TSV, signal integrity.

I. INTRODUCTION

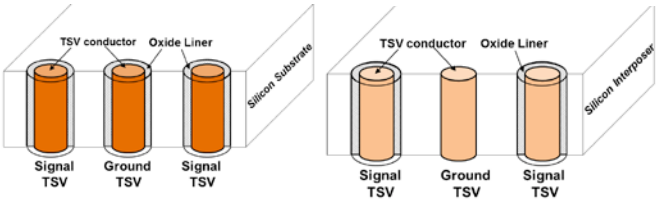
A 2.5D integration approach, the silicon interposer based on through silicon via(TSV) interconnects enables the high-density integration of multiple IC dies. However, the crosstalk between the signaling TSVs is of vital important due to the short pitch between parallel TSV interconnects through which the digital signal is transmitted, and a considerable amount of studies have been performed in the past [1-6].

One effective approach for crosstalk mitigation is to insert the ground TSVs on the periphery of signal TSVs. The effect of ground TSVs on crosstalk has been studied in [3], and the thermal effects on TSV crosstalk has been investigated in [8]. In conventional design, the signal and ground TSVs utilize an oxide layer to separate TSV metal conductors and silicon substrate. This oxide layer forms the metal-oxide-semiconductor (MOS) structure of TSVs. As a consequence, an extra oxide capacitance and MOS capacitance are formed between the ground/signal TSVs and silicon substrate [2, 4, 9, 13]. Such capacitances, which is frequency-dependent, can reduce the effects of the ground TSVs on crosstalk mitigation. In [6], the electrical design and physical-based frequency-domain modeling of a new signal-ground-signal (SGS) TSV signaling scheme where the ground TSVs without oxide liner have been proposed for 3D stacked chips. However, the proposed model in [6] assumes perfect ohmic contact [14] for the metal-silicon interface of a ground TSV. As a result, the contact resistance for metal-silicon interface and the effect of doping concentration on crosstalk are not taken into account. In addition, as the silicon substrate for IC dies is usually grounded and has zeros potential, the direct ohmic contact for ground TSV may not be necessary. In [15], we have rigorously analyzed the contact resistance and shows that the contact resistance may affect the performance of this isolation effect. And for multi-TSV structures, the ground TSV without oxide liner needs to be analyzed.

In this paper, we investigate the time domain performance of the multi TSV signaling scheme with ground TSVs directly contacting the silicon substrate. The paper is organized as follows: in Section II, the performance of time domain using ground TSVs without oxide liner compared to the original scheme is introduced. In Section III, the crosstalk of multi-TSV using new scheme are presented. The effect of the new design on multi-TSV crosstalk and noise coupling are discussed. The conclusion is summarized in Section IV.

II. CONDITION ANALYSIS FOR SGS SCHEME

Fig.1b shows a SGS scheme where the TSV conductor is directly contacted with silicon-substrate in the ground TSV. The crosstalk performance is analyzed in both frequency and time domains, where the TSV diameter, length, and oxide insulator layer thickness are 20, 100, and 0.1 μm , respectively. The pitch between TSVs is 50 μm . p-type silicon substrate, and the material parameters at 300 K are used. The silicon conductivity is 10 S/m, and the substrate doping concentration is 1.2e+15 cm^{-3}. The calculated threshold voltage V_T is 0.604 V.



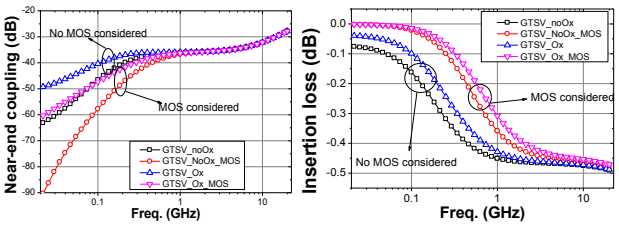
(a) (b)

Fig. 1. SGS structures using Gound TSV (a) with and (b) without oxide liner.

A. Crosstalk with and without Considering MOS Effect and the Condition discussion of MOS Effect

Because of the induced MOS capacitance for TSVs [2,4,9,13,15], the effect of MOS capacitance on signal crosstalk is investigated. Fig. 2a shows the crosstalk comparison with and without MOS capacitances for both new

and conventional schemes. It shows that the crosstalk decreases when MOS capacitance is considered, compared to the case without MOS capacitance. In addition, it also shows that even with MOS capacitance, the ground TSV direct contacts silicon interposer via ohmic contact can provide lower crosstalk, compared to the case using insulator-coated ground TSV. In other words, the inclusion of MOS capacitance does not change the trend for the near-end coupling. As the MOS capacitance is in series with the oxide capacitance, the total equivalent capacitance becomes lower, compared to the case without MOS capacitance. Therefore, the curves shift to higher frequency, compared to the case without considering MOS capacitance (Fig. 2a). Fig. 2b shows the insertion loss considering MOS capacitance. It shows that compared to the case without considering MOS capacitance, less insertion loss is obtained when MOS capacitance is considered. As one signal TSV is an aggressor TSV and the other signal TSV is the victim TSV in time domain (Fig. 4), different depletion thicknesses are required for the aggressor TSV and the victim TSV. Using same depletion thickness for both signal TSVs can lead to discrepancy, as shown in Fig. 3.



(a) (b)

Fig. 2. (a) Near-end crosstalk, (b) insertion loss comparisons with and without MOS capacitance.

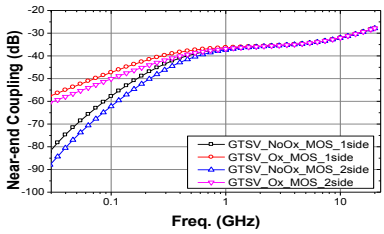


Fig. 3. Crosstalk comparison with even and uneven MOS depletion region. (1side: 1 port is excited with high frequency 0-1.8V transmitting signal; 2side: 2 ports are both excited with high frequency 0-1.8V transmitting signals.)

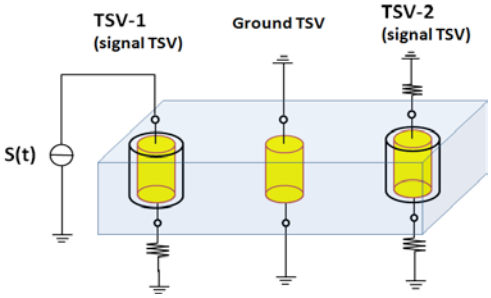
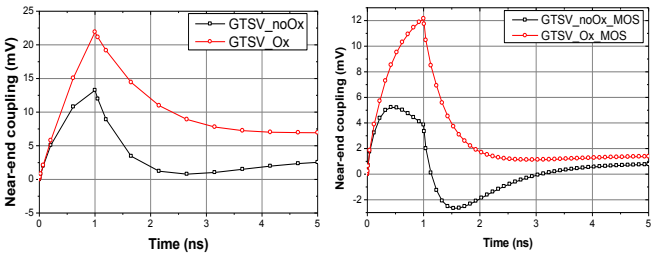


Fig. 4. Time-domain simulation configuration for the SGS structure.



(a) (b)

Fig. 5. Near-end coupling and transmitted signal with 1 ns rise time: (a) without considering MOS effect, (b) considering MOS effect.

B. *Time Domain Characteristics*

As the coupled noise can affect the signal integrity in time-domain, we investigate the effects of ground TSV and MOS capacitance on time-domain coupled noise coupling for both the novel and the conventional schemes. The time domain models are built based on the wideband simulation results in the frequency domain. The time-domain simulation configuration is shown in Fig. 4. One input signal is transmitted on signal TSV-1. All other terminals of signal TSV-1 and TSV-2 are terminated using a 50 Ohm resistor. The TSV in the middle, a ground TSV, is shorted to ground.

1) *Coupling with Step Input Signal*

TABLE I. TIME AND MAGNITUDE COMPARISONS WITH 100 MHZ CLOCK SIGNAL AND 1 NS RISE TIME.

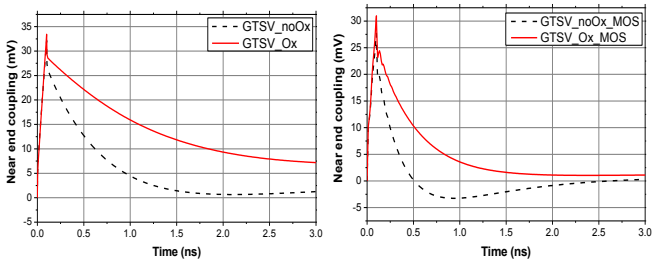
		New Design	*Conventional Design*	*Reduction (%)*
No MOS Effect	Peak Value (mV)	13	22	40.9%
	Pulse Width (ns)	1.02	1.6	36.2%
With MOS Effect	Peak Value (mV)	5.4	12.1	55.4%
	Pulse Width (ns)	0.87	1.1	20.9%

TABLE II. TIME AND MAGNITUDE COMPARISONS WITH 1 GHZ CLOCK SIGNAL AND 100 PS RISE TIME.

		New Design	*Conventional Design*	*Reduction (%)*
NO MOS Effect	Peak Value (mV)	32	33	3.3%
	Pulse Width (ns)	0.27	0.85	68.2%
With MOS Effect	Peak Value (mV)	26	29	10.3%
	Pulse Width (ns)	0.2	0.37	45.9%

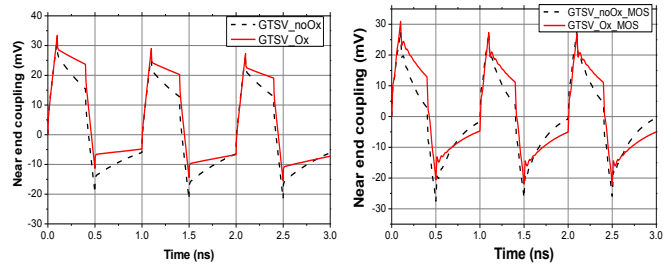
First, we use a step signal with rise time of 1 ns as the input signal S(t) on signal TSV-1. The magnitude of the input signal is 1.8 V. The simulated near-end coupled noise on TSV-2 and transmitted signal on TSV-1 are shown in Fig. 5. Fig. 5 shows that for both cases with and without considering MOS effects, the new scheme using ground TSV without oxide layer can reduce the coupled noise on TSV-2, compared to the conventional design. This validates the effectiveness of the ground TSV with ohmic contact on crosstalk. The time and magnitude comparisons are shown in Table 1 for the cases with and without MOS effect. In Table 1, the pulse width (PW) represents the time interval between the rising edge and falling edge of the pulse at the point where its amplitude is

50% of its peak value. As shown in Table 1, the new scheme can reduce the PW by 36.2% and 20.9% for the cases without MOS effect and with MOS effect, respectively. Table 1 also shows that without considering MOS effect, the peak noise is 22 mV for the conventional design. However, the noise is reduced by 13 mV using the new scheme, about 41% reduction. Considering the MOS capacitance, the peak noise is 12.1 mV for the conventional design. However, the noise is reduced by 5.4 mV using the new scheme, about 55.4% reduction. For the transmitted signal on TSV-1, Fig. 5 shows that using the new scheme, the signal magnitude is reduced about 1.2 mV and 0.7 mV for the cases without and with MOS effect, respectively. The reduction in magnitude is due to the fact the new scheme has slightly larger insertion loss than the conventional approach, as shown in Fig. 5.



(a) (b)

Fig. 6. Near-end coupling and transmitted signal with 100 ps rise time, (a) without considering MOS effect, (b) considering MOS effect.



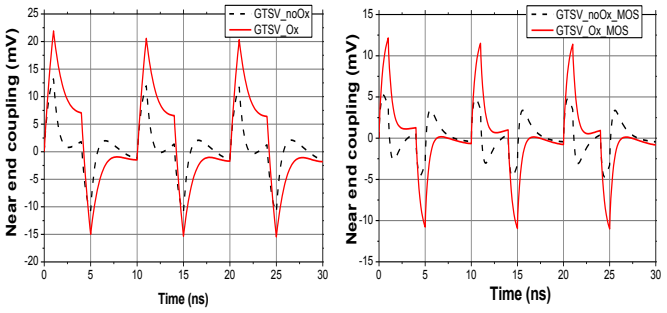
(a) (b)

Fig. 7. Coupled noise with 1 GHz clock signal (the rise and fall time of transmitted signal are both 100ps), (a) without considering MOS effect, (b) considering MOS effect.

Secondly, we use a step signal with rise time of 100 ps as the input signal S(t). The magnitude is kept as 1.8 V. The near-end coupled noise on TSV-2 and the transmitted signal is shown in Fig. 6. The time and magnitude comparisons are shown in Table 2. Compared to the conventional design, although the coupled peak noise is reduced only 2.2 and 1.1 mV for the cases without MOS effect and with MOS effect, the new scheme can reduce the pulse width by 68.2% and 45.9% for both the cases without MOS effect and with MOS effect, respectively. The reduced PW indicates that the noise amplitude decrease quickly using the new scheme. For example, Fig. 6a shows that at 1 ns, the coupled noise is reduce to 5 mV for the new scheme while the noise is about 16 mV for the conventional design.

2) Coupling with Periodic Input Signal

We also simulate the coupled noise with periodic clock signal as input signal *S(t)*. The magnitude of the input signal is also 1.8 V, and the duty ratio is 50%. The thickness of the calculated depletion region for TSV-1 with periodic signal excitation is 0.68 micron. As the crosstalk signal on TSV-2 is very small, the calculated depletion thickness is 0.27 micron for both TSV-2 and the ground TSV. Using 1 GHz clock signal with 100 ps rise and fall time, the coupled noise waveforms are shown in Fig. 7a and Fig. 7b, respectively. Using 100 MHz clock signal with 1 ns rise and fall time as input signal, the coupled noise waveforms are shown in Fig. 8a and Fig. 8b, respectively. As shown in Fig. 8, the new scheme can reduce the coupled peak noise dramatically, compared to the conventional design.



(a) (b)

Fig. 8. Coupled noise of 100 MHz clock signal (the rise and fall time of transmitted signal are both 1ns), (a) without considering MOS effect, (b) considering MOS effect.

III. MULTI-TSV SCHEME

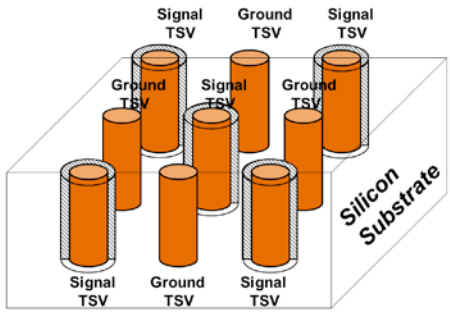


Fig. 9. 3X3 TSV array structure.

In this section, we analyze a 3x3 TSV array to investigate the performance of multi TSV array using ground TSV directly contact to silicon interposer compared to original structures shown in Fig. 9. The TSV diameter, length, and oxide insulator layer thickness are 20, 100, and 0.1 μm, respectively. The pitch between TSVs is 50 μm. For comparison, the convectional design with insulator-coated ground TSV is also simulated. The silicon is the same as that in Section II. Because the MOS effect does not affect the trend of performance as shown in Section II, we omit the MOS effect in this analysis.

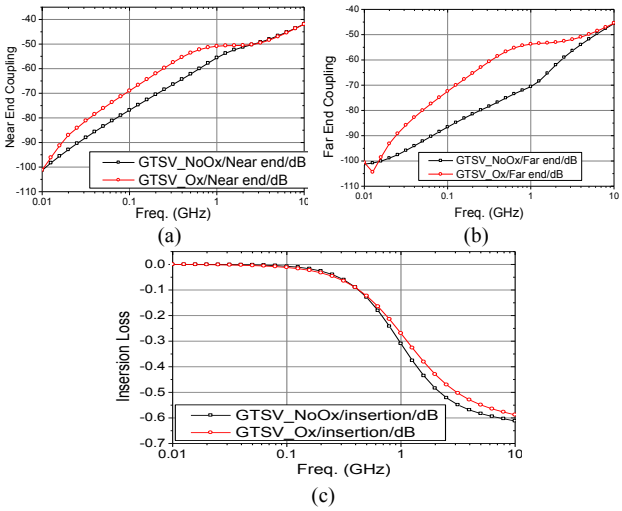


Fig. 10. (a) Near end coupling and (b) Far end coupling between corner signal TSV and another neighbor-side corner signal TSV; (c) Insertion loss of each corner TSVs.

The crosstalk and insertion loss comparisons are shown in Fig. 10 for the cases in which the ground-TSVs are coated with and without oxide liners. In Fig. 10a and 10b, the proposed scheme performs better far end and near end coupling between two neighbor signal TSVs on each side. There is approximately 10dB lower coupling than the conventional structures from 20MHz to 1GHz. The coupling between center signal TSV and corner signal TSV also gives the similar performance. The reduction of coupling is about 10dB from 20MHz to 0.9GHz. However, there is little insertion loss decrease. The insertion loss reduces within 0.1dB from 10MHz to 10GHz, and this tiny loss is acceptable compared to the coupling reduction.

IV. CONCLUSION

In this paper, a crosstalk-reduction signaling scheme using ground TSVs directly contacting silicon interposer to reduce the crosstalk is analyzed in time domain, and it is further expanded this structure to multi TSV array. The effects of the scheme and MOS capacitance on crosstalk are investigated using simulations in both frequency and time domains. The simulation results demonstrate that the new grounding scheme can effectively reduce the crosstalk, compared to the conventional scheme using insulator coated ground TSVs in multi TSV array applications.

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