

Measurement and Analysis of Wireless Power Distribution Network using Magnetic Field Resonance in 3D Package and IC

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Abstract—To overcome power distribution network (PDN) design challenges such as serious power noise, large system area burden, the wireless power transfer (WPT) system in the 3D package and IC is applied. In this study, the 3D multi-helix inductor is proposed for designing the 3D package and IC with a WPT scheme and an equivalent circuit modeling is also implemented. The fabricated package WPT system represents a voltage transfer ratio (VTR) of 77.4 % and a system-level power efficiency of 53.0 %. The wireless PDN impedance is analyzed to verify the performance of the 3D package and IC with a WPT scheme in terms of SSN. It shows excellent performance in terms of SSN because the DC voltage output section of the rectifier of the WPT system can be assumed as voltage regulator module (VRM). Also, it has a characteristic of a band-pass filter (BPF), which passes resonance frequencies only due to the magnetic field resonance characteristic of WPT. Thus, the 3D package and IC with a WPT scheme becomes an excellent PDN solution that can reduce such system area burden and power noise at the same time.

Keywords— wireless power transfer, wireless power distribution network, 3D package and IC, magnetic field, resonance, inductor design, power efficiency, simultaneous switching noise.

I. INTRODUCTION

The 3D package and IC enable wide I/O based high electrical performance, low power consumption, small form factor, and low cost requirements of the next generation of electronic devices. In particular, as the 3D package and IC can implement wide I/O using TSV technology, it can be used as a solution of high performance mobile devices, such as AP (application processor), DDR (double data rate), and DRAM (dynamic random access memory), that requires a system bandwidth of hundreds of GBs. In spite of such advantages, 3D system integration represents lots of switching I/O pins in order to implement wide I/O and that is vulnerable to power noise such as simultaneous switching noise (SSN). Thus, the system area burden is also increased according to increases in distributing both many decoupling capacitors for reducing such power noise and TSVs for presenting the wide I/O in the 3D package and IC. Therefore, a new PDN solution is required to reduce not only the power noise, but also the system area burden in the 3D package and IC. The wireless

power transfer (WPT) is a technology that transfers power wirelessly through an inductive decoupling method without using power interconnections, such as package balls and bumps, to power lines. The WPT technology has already been applied to various fields including smart phones, electric vehicles, bio-medicals, energy harvesting, and so on [1],[2]. Moreover, studies on the magnetic field resonance based WPT have largely been conducted as a technology that transfers power or signals wirelessly in the 3D package and IC. In this study, a WPT scheme is proposed as a solution for reducing not only the power noise, but also the system area burden in the 3D package and IC. It is possible to reduce power TSVs, power balls, and power bumps through applying WPT to the 3D package and IC and that leads to minimize the system area burden. In addition, the power noise can be filtered by implementing the WPT technology for the 3D package and IC in terms of the power noise. Therefore, in this study the WPT scheme is implemented in the 3D package and IC and the voltage transfer and power efficiency in WPT are analyzed. Also, the wireless PDN characteristic (Z_{11}) of the 3D package and IC, which applies WPT in terms of SSN, is analyzed. Moreover, it will be verified by measuring the band-pass filter (BPF) characteristic of WPT using magnetic field resonance.

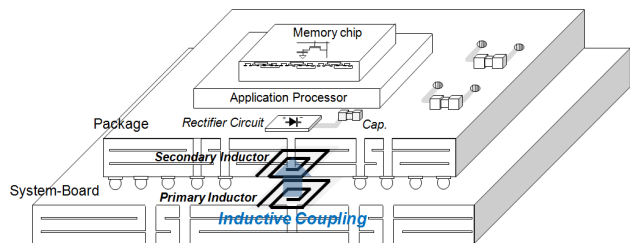


Fig. 1. System board-to-package wireless power transfer system using magnetic field resonance

Fig. 1 shows the system board-to-package wireless power transfer scheme, which uses magnetic field resonance. WPT scheme used in this paper is a power transfer method using the magnetic field resonance between the primary and secondary inductors. A rectifier circuit such as a diode is required next to the secondary inductor to convert the transferred AC power to

DC. For analyzing the SSN characteristics in the 3D package with a WPT scheme presented in Fig. 1, the wireless PDN impedance is introduced. Therefore, for analysing the 3D package with a WPT scheme in terms of SSN, a new schematic definition of the wireless PDN different from the conventional wired PDN is required.

II. INDUCTOR MODELING AND DESIGN OF WIRELESS POWER TRANSFER SYSTEM IN A 3D PACKAGE

In order to demonstrate the wireless PDN performance in a 3D package, which has a WPT scheme, a BGA package is designed using magnetic field resonance. First of all, it is necessary to optimize the inductor structure suitable for 3D package. The size of the BGA package is configured as 35 mm×35 mm and the package PCB is composed of four layers. Thus, the inductor size is determined as 10 mm×10 mm for implementing the inductor to the BGA package. Fig. 2 shows the proposed 3D multi-helix inductor. As shown in Fig. 2, the inductor was designed using a multi-layer PCB for increasing the inductance of the inductor, while maintaining a small size in the package.

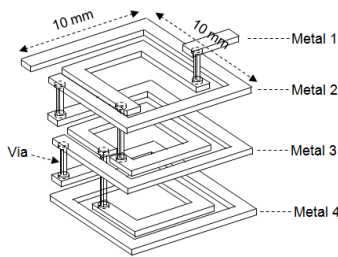


Fig. 2. Design and structure of the 3D multi-helix inductor in a 3D package for analysing the wireless PDN.

For optimizing the structure of the proposed 3D multi-helix inductor, the equivalent circuit modeling is performed.

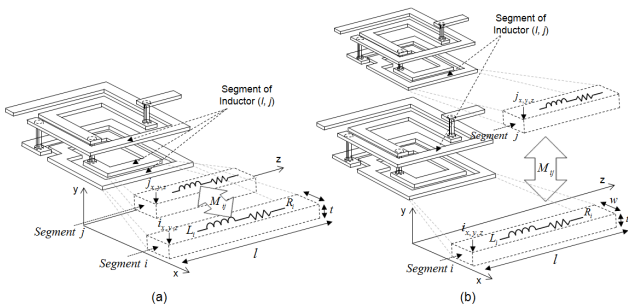


Fig. 3. Model of the static parasitic resistance (R) and the self inductance (L) of segment i and the mutual inductance (M); (a) between segments i and j of an inductor (b) between segments i and j of inductors on 3D package and IC.

Fig. 3 depicts the static parasitic resistance (R), the self (L) and mutual (M) inductances of the segments of multi-helix inductors. A segment of inductor is defined as a metal strip of inductors. The static parasitic resistance of each segment of

the multi-helix inductor is easily calculated from the sheet resistance of the metal traces. The static self inductance can be defined in integral form by Eq. (1).

$$L_i = \frac{\mu}{4\pi} \frac{1}{t^2 w^2} \iint_{A_i A_i'} \iint_0^{l_i'} \frac{|dl_i dl_i'|}{r_{ii'}} dA_i dA_i' \quad (1)$$

where dA_i and dA_i' are both the area of infinitely small filaments in the segment i .

For the calculation of the mutual inductance between segments in the same level or on multiple levels, Eq. (2) is used. As an example, Eq. (2) calculates the mutual inductances between the segment i and j , M_{ij} , by summing the self inductances of 64 virtual segments defined by combinations of two corner points ($i_{x,y,z}$, $j_{x,y,z}$) of segments i and j [3]. $i_{x,y,z}$, $j_{x,y,z}$ are one of the eight corner points of each segment. Eq. (2) gives accurate mutual inductances over a wide range of dimensions because it is based on the self inductance (L_i) calculation.

$$\begin{aligned} M_{ij} &= \frac{1}{A_i A_j} \iint_{A_i A_j} M_{dA_i dA_j} dA_i dA_j \\ &= \frac{1}{w_i l_i w_j l_j} \int_{x_{i0}}^{x_{i1}} \int_{x_{j0}}^{x_{j1}} \int_{y_{i0}}^{y_{i1}} \int_{y_{j0}}^{y_{j1}} \left[\frac{\mu}{4\pi} \int_{z_{i0}}^{z_{i1}} \int_{z_{j0}}^{z_{j1}} \frac{1}{r} dz_i dz_j \right] dy_i dy_j dx_i dx_j \\ &= \sum_{x,y,z \in \{0,1\}} L_{i_x, y_y, z_z} j_{x,y,z} \end{aligned} \quad (2)$$

Fig. 4 shows the comparison of the PDN impedance (Z_{11}) between the proposed multi-helix equivalent circuit model and the 3D field solver (HFSS). As shown in Fig. 4, the PDN impedance of the proposed equivalent circuit model agrees well with an EM simulation. Regarding the PDN impedance, resonances presented at the frequency band over 200 MHz are caused by the LC resonance between the segments of the multi-helix inductor. Thus, it does not appear in a lumped equivalent circuit model.

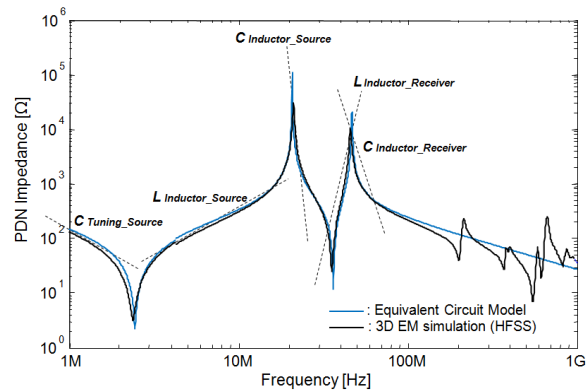


Fig. 4. Comparison and analysis of the PDN impedance (Z_{11}) between the equivalent circuit model and 3D EM simulation (HFSS) for the inductor-to-inductor system.

To locate a 3D multi-helix inductor at the center of the package in the bottom layer, package balls are placed only by two lines at the outer block of the package. The package body

size is designed as 35 mm×35 mm and the package balls consist of signal and ground balls.

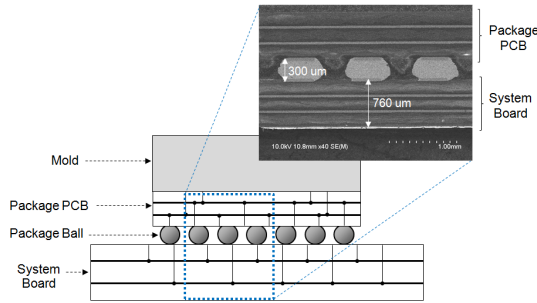


Fig. 5. SEM images of the system board-to-package WPT system.

Fig. 5 shows the scanning electron microscope (SEM) images of the system board-to-package WPT system in which the distance between the system board and package is 300 μm, which is equal to the height of package balls. Since a transfer distance in the package-level WPT is very short as determined as 300 μm, the magnetic field can be tightly coupled. In order to verify the performance of the practically fabricated WPT system, the measurement of its power efficiency was carried out. A sinusoidal voltage of 2.5 MHz is applied to the system board (TX) from a signal generator, and AC power is transferred to the package (RX) through inductive coupling. Then, DC power can be obtained after the rectifier circuit.

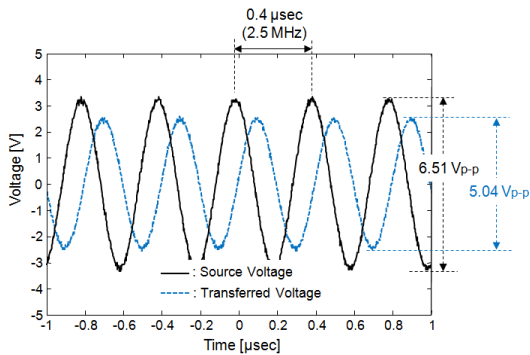


Fig. 6. Comparison of the measured voltage between the source and transferred powers for the inductor-to-inductor voltage transfer ratio.

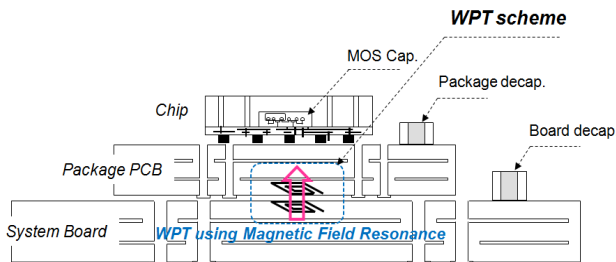


Fig. 7. Structure of the hierarchical system board-package-chip PDN with a WPT scheme using magnetic field resonance.

The multi-helix inductor used in the package is designed as a dimension of 10 mm×10 mm, metal width of 300 μm, and

4.5 turns of inductor winding. Also, the parameters of the multi-helix inductor are calculated using a 3D EM field simulator (Ansys, HFSS). The calculated self and mutual inductance in the multi-helix inductor are 2.045 and 1.278 μH respectively.

III. WIRELESS PDN ANALYSIS OF THE 3D PACKAGE-LEVEL WPT SYSTEM

For analysis of the property of the wireless PDN in a 3D package system, a hierarchical system board-package-chip PDN is proposed as illustrated in Fig. 7. Table I shows the key design parameters in the hierarchical PDN of a 3D package, which has a WPT scheme. The design parameters are used to analyze the wireless PDN impedance characteristic.

TABLE II. DESIGN PARAMETERS FOR THE HIERARCHICAL SYSTEM BOARD-PACKAGE-CHIP PDN IN A 3D PACKAGE WITH A WPT SCHEME.

DESIGN PARAMETERS	VALUES	DESIGN PARAMETERS	VALUES
System board dimension	60 mm × 60 mm	Chip size	2 mm × 2 mm
Decaps on the system board	100 nF, (ESL=1.5 nH)	MOS decaps in chip	900 ea (Cox = 0.815 pF, ESR = 17.65 Ω / decap)
Package body size	35 mm × 35 mm	Bump ESL	200 pH
Package decaps	10 nF, (ESL=0.5 nH)	Package ball ESL	500 pH

Fig. 8 represents the comparison result between the conventional hierarchical PDN that includes MOS capacitors, and package and system board decaps and the hierarchical PDN in which a WPT scheme is added. It shows that a design of low hierarchical PDN impedance can be performed using the conventional decoupling solution in the 3D package and IC.

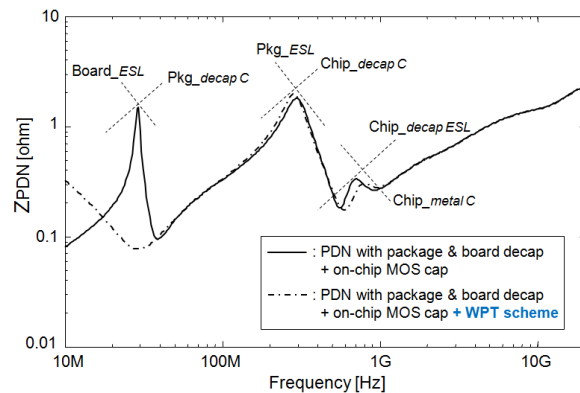


Fig. 8. PDN impedance comparison for the conventional hierarchical PDN and the proposed wireless PDN solution.

However, if the WPT scheme is included in the 3D package and IC, the influence of the system board will not be presented due to the reverse characteristic of the system board. As a

result, with the WPT scheme added closer to chips, the parallel resonance peak of the PDN impedance is decreased due to the reverse characteristic in the diode.

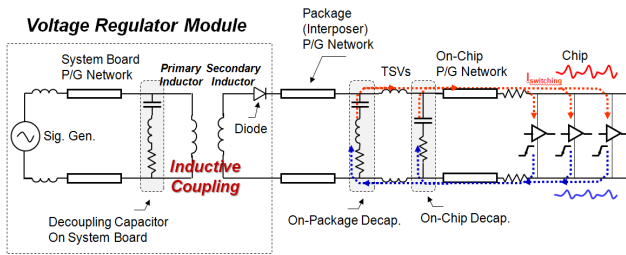


Fig. 9. New definition for the schematic of a power distribution network (PDN) for 3D package and IC with WPT scheme.

Fig. 9 represents the new schematic for defining the PDN in a package-level WPT system in terms of SSN. The most important difference between the conventional wired PDN schematic and the wireless PDN schematic is the use of inductive coupling. In this paper, variations in the PDN impedance property are analyzed in terms of SSN for wireless PDN with inductive coupling. As the ripple voltage of the DC power in a rectifier circuit is very small, considering it as ideal DC power, the PDN from the system board to the rectifier circuit can be simplified as a voltage regulator module (VRM).

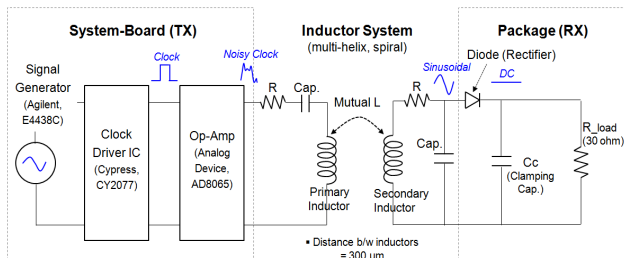


Fig. 10. System configuration for analyzing the noise filtering property of the package-level WPT.

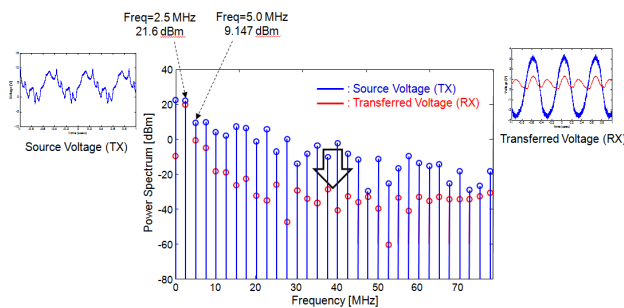


Fig. 11. Comparison and analysis of the power spectrum between the source and transferred voltages.

Fig. 10 shows the system configuration for analyzing the power noise filtering characteristic of the package-level WPT system. In order to generate noisy clock signals at the system board (TX), the sinusoidal signals generated from a signal generator are transformed to clock signals through a clock

driver and an op-amp is used to amplify noisy clocks. The WPT system basically represents a characteristic that well transfers only the resonance frequency components and filters other frequency components. Thus, the proposed package-level WPT system can function as BPF that reduces the power noise of PDN in a 3D package. Fig. 11 shows the comparison of the power spectrum between the measured source and the transferred voltage in the package-level WPT system. As shown in Fig. 11, the frequency component of 2.5 MHz, which is the resonance frequency of WPT is well transferred only and other frequency components are filtered.

IV. CONCLUSION

In this study, the 3D package and IC that overcomes design challenges such as SSN and system area burden in a 3D stacking structure is proposed. For applying the WPT scheme to the 3D package and IC, a multi-helix inductor structure, which has a small size, 10 mm×10 mm, was designed. The WPT system in the 3D package and IC represents the voltage transfer ratio and power efficiency of 77.4 and 53 %, respectively. Using the WPT scheme it is possible to minimize the system area burden in the 3D package and IC by reducing the power TSVs and power balls. Also, the power noise such as SSN can be reduced using the characteristic of the WPT system. A new PDN schematic with the WPT scheme is proposed and the wireless PDN impedance is also compared and analyzed in terms of SSN. The WPT-based hierarchical PDN shows a bit more advantageous characteristic in terms of power noise compared to that of the conventional interconnection-based hierarchical PDN. The proposed package-level WPT system is a desirable wireless PDN solution to reduce a system area burden and power noise caused in a 3D package and IC that represents a system bandwidth of hundreds of GBs. In addition, if an interposer or a chip-level WPT scheme is implemented in 3D packages and ICs, it is expected to present more excellent PDN impedance property.

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REFERENCES

- [1] Guoxing Wang, Wentai Liu, M. Sivaprakasam, G.A. Kendir, "Design and analysis of an adaptive transcutaneous power telemetry for biomedical implants," *IEEE Transactions on Circuits and Systems*, vol. 52, no. 10, pp. 2109-2117, 2005.
- [2] M.A.R. Khan, *et al.*, "Wireless power transfer: An application to cell phone battery recharging," *15th International Conference on Computer and Information Technology (ICCIT)*, pp. 305-309, 22-24 Dec. 2012.
- [3] Z. Guoan, K. Cheng-Kok, "Exact closed-form formula for partial mutual inductances of rectangular conductors," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol.50, no.10, pp. 1349- 1352, Oct. 2003.