A low cost capacitor approach for suppressing resonance in power distribution networks

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***Abstract*—Resonances in power distribution network are the major cause of voltage fluctuation and noise problems. In this paper, a new method that suppresses impedance peak is proposed. The proposed method uses a high series resistance (HSR) capacitor in parallel to regular bypass capacitors. By selecting the parameters so that the series resonance frequency of the HSR capacitor equals to the anti-resonance frequency of the bypass capacitors, current path will be formed through the HSR capacitor, suppressing the impedance peak. Relatively low required capacitance in this configuration enables low cost fabrication of the HSR capacitor. Experimental measurements using a double-side printed circuit board have shown that the proposed method lowers the peak impedance by 10-fold and reduces radiation noise by 10 dB.**

I. Introduction

Design constraint for voltage fluctuation in power distribution network (PDN) has become even severer as the progress of CMOS process technology. The performance improvements of integrated circuits have increased power consumption, and hence the chances of having large voltage fluctuation increases. The design of low impedance PDN that satisfies a target PDN impedance is a critical criteria for ensuring power integrity [1].

A mesh-like equivalent circuit model is widely used to represent power and ground planes in package interposer and printed circuit board (PCB). Wires, through-holes, and passive components are typically modeled as inductors, capacitors and resistors as shown in Fig. 1. A network of energy-storing circuit elements induces peaks of PDN impedance due to parallel resonance. Reduction of the peaks is the main objective to satisfy a given target impedance [2,3]. Moreover, the peak impedance due to parallel resonance is often the source of EMI problems when the resonance frequency matches to the harmonics of the clock signal [1]. Hence, the reduction of the maximum impedance of PDN circuits is one of the most important objectives in the PDN circuit design.

At board-level designs, there are two major countermeasures taken to mitigate the high PDN impedance. One is to use many bypass capacitors, which have low series resistance (LSR), in parallel. The other is to use capacitors that have high series resistance (HSR). Here, the LSR capacitor is an ordinary multi-layer ceramic capacitor (MLCC) that is designed to minimize equivalent series resistance (ESR). On the other hand, the HSR capacitor is the one that is given an intentional series resistance by design. In the first method, the quality factor of the resonance is improved. Hence, this method lowers impedance, but essentially does not reduce the peak impedance. The second method reduces the quality factor, so does the peak impedance, but it has the side-effect to increase low frequency impedance [3]–[5].

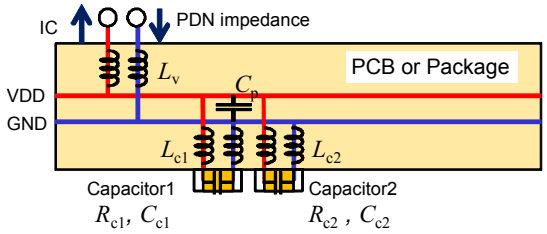

Fig. 1. Typical circuit model for the power distribution network of an electrical system.

In [6], yet another approach is proposed, in which the LSR and HSR capacitors are used in a pair. This method is effective in reducing the maximum impedance at a parallel resonance frequency without increasing the impedance at low frequencies. However, there is a cost issue for the HSR capacitor. Its capacitance has to be large (usually larger than 0.1 μF) to match the value with normal bypass capacitors. Many layers of internal electrodes are required to achieve the large capacitance value, which makes it difficult to fulfill the high resistance requirement by the internal electrodes. Thus, the HSR is realized by adding a high-resistance metal as external electrodes, which is very costly.

In this paper, we propose a new method to reduce the impedance peak of the PDN due to parallel resonance. Our method also uses HSR capacitor, but its capacitance can be small so the series resistance is achieved by the internal electrodes only. We experimentally show that the proposed method reduces the peak impedance and radiation noise effectively as compared to the conventional methods.

II. Suppression of anti-resonance impedance

A. Conventional methods

We first review conventional methods by using a simple PDN structure in Fig. 1. Figure 2 shows its equivalent circuit. Here, parasitic resistances and inductances of power and ground planes are ignored. $L_{\rm v}$ is the parasitic inductance between LSI and PDN plane, and $C_{\rm p}$ is the capacitance of the PDN plane. $C_{\rm c1}$, $L_{\rm c1}$, $R_{\rm c1}$ and $C_{\rm c2}$, $L_{\rm c2}$, $R_{\rm c2}$ are the capacitance, inductance and resistance of the two bypass capacitors.

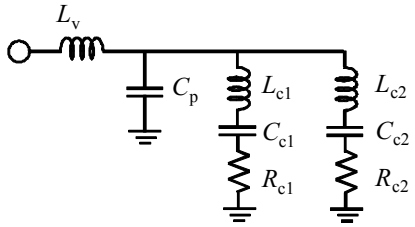

Fig. 2. Simple equivalent circuit of the power distribution network in Fig. 1.

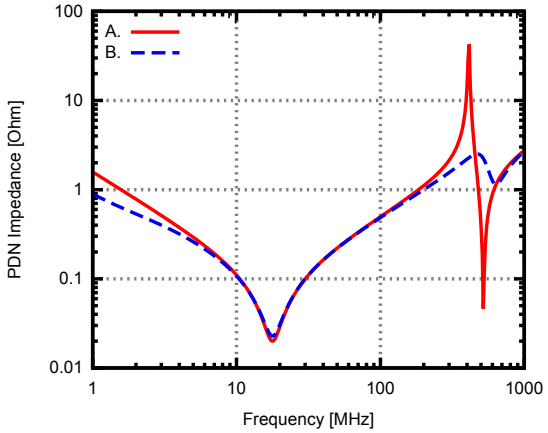

Fig. 3. PDN impedance using conventional methods: only the LSR bypass capacitors are used (A) and both LSR and HSR capacitors are used (B).

TABLE I
CIRCUIT PARAMETERS IN FIG. 3.

Cond-ition	L_v [nH]	C_p [pF]	Capacior 1 C_{c1} [μF]	L_{c1} [nH]	R_{c1} [mΩ]	Capacitor 2 C_{c2} [μF]	L_{c2} [pH]	R_{c2} [mΩ]
A	500	500	0.1	300	10	-	-	-
B	500	500	0.1	300	10	0.1	300	1000

In the conventional method [6], LSR and HSR capacitors, which have equal ESL and capacitance, are mounted in parallel. An example impedance curves are shown in Fig. 3. Lines A and B show the impedances when only the LSR bypass capacitors are used and when both LSR and HSR capacitors are used, respectively. Table I shows circuit parameters for each case. The simultaneous use of the LSR and HSR capacitors that have equal ESL and capacitance means both types of capacitors have equal frequencies of series and parallel (anti-) resonance. As a result, at the anti-resonance frequency, peak impedance is determined by that of the HSR capacitor because the current flows in the low impedance path. Here, the maximum effectiveness is obtained when the HSR satisfies the following equation [6].

$$R_{c2} = \omega L_{c2} \tag{1}$$

B. Proposed method

The conventional method reduces the PDN impedance by enforcing anti-resonance frequencies of LSR and HSR capacitors equal [6]. In contrast, the proposed method matches the anti-resonance frequency of the LSR capacitor to be equal to the series-resonance frequency of the HSR capacitor to reduce peak impedance. Here, anti-resonance of LSR capacitor occurs between ESL L_{c1} and the parasitic capacitance of the PDN plane C_p. Series resonance of HSR capacitor occurs due to L_{c2} and C_{c2}. Hence, to match the series resonance frequency with anti-resonance frequency, the following equation should be satisfied.

$$2\pi\sqrt{L_{c1}C_p} = 2\pi\sqrt{L_{c2}C_{c2}} \tag{2}$$

Assuming that the ESLs of the two capacitors are equal, resonance frequency can be made equal by choosing capacitor 2 to be $C_{c2} = C_p$.

Figure 4 shows the impedance when regular LSR bypass capacitors (condition A) and the LSR capacitor that satisfies $C_{c2} = C_p$ are used (condition C). The line A in Fig. 3 is re-plotted here for comparison. Table II shows the circuit parameters used to draw Fig. 4. Condition C now has two parallel resonances: on the higher and the lower frequencies of the parallel resonance of condition A. The anti-resonance in lower frequency is caused by the ESL of capacitor 1 and C_{c2} because capacitor 2 is in series resonance and its reactance is very small. Similarly, the anti-resonance in higher frequency is caused by the ESL of capacitor 2 and PCB plane capacitance C_p since capacitor 2 is inductive at this frequency.

The two anti-resonances can be suppressed by increasing ESR of the bypass capacitors — because the anti-resonaces are both caused by the LSR capacitors. Figure 5 shows the case when an HSR capacitor that satisfies $C_{c2} = C_p$ is used (line D). The two peaks are flattened as compared with condition C, which is the re-plot of Fig. 4.

Because there are two anti-resonance frequencies, obtaining a closed-form equation of the optimal series resistance for the low capacitance capacitor is difficult. The optimal parameters for an HSR capacitor are obtained by solving the following simultaneous equations based on a simple PDN model in Fig. 2.

$$\begin{cases} \omega &= f(R), \\ Z_{\max} &= g(\omega, R). \end{cases} \tag{3}$$

Here, R is an ESR of the HSR capacitor, ω is the anti-resonance angular frequency that is dependent on the parameter of the HSR capacitor, and $Z_{\max}$ is the peak impedance at the antiresonance. Other parameters in Table II are also in the equations but omitted for the sake of simplicity. The functions f and g are too complex for analytical calculations, but Eq. (3) can be numerically evaluated by using circuit simulations. By finding R that gives the smallest $Z_{\max}$, optical ESR for the HSR capacitor can be calculated.

TABLE II
CIRCUIT PARAMETERS IN FIGS. 4 AND 5.

Cond-ition	L_v [nH]	C_p [pF]	Capacitor 1 C_{c1} [μF]	L_{c1} [nH]	R_{c1} [mΩ]	Capacitor 2 C_{c2} [pF]	L_{c2} [pH]	R_{c2} [mΩ]
A	500	500	0.1	300	10	-	-	-
C	500	500	0.1	300	10	500	300	10
D	500	500	0.1	300	10	500	300	1000

III. EXPERIMENTAL VERIFICATION

We verify the proposed method through experiments using a double-sided board that mimics a PDN circuit. Figure 6 shows

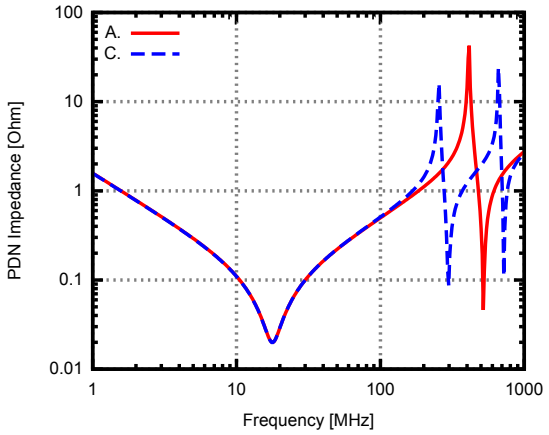

Fig. 4. PDN impedances: both LSR and HSR capacitors are used (B), and LSR and low capacitance capacitor is used (C).

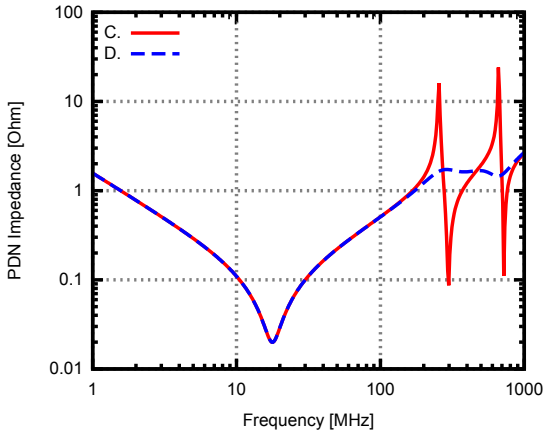

Fig. 5. PDN impedances: LSR and low capacitance capacitor is used (C), and HSR and low capacitance capacitor is used (D).

a construction of the evaluation board. The thickness of the board is 1.6 mm. There are VDD and GND patterns on the top and the bottom layers, respectively. An SMA connector is mounted at the bottom layer to connect VDD pattern through via hole. In order to alter capacitance and its series resistance arbitrarily, the series connection of a ceramic capacitor and an SMD resistor are considered as an ESR-changeable capacitor. Table III shows the parameters of capacitors. The parameters are determined to correspond to the ones in Section II. In all conditions, capacitor 1 is composed of the combination of a 0.1 μF ceramic capacitor and a short resistor. The resistance 50 mω is the total ESR determined by the measurement. The capacitance of 39 pF in conditions C and D is determined by the measurement of the plane capacitance of the board. The resistance values in conditions B and D are roughly determined by Eq. 1 and then experimentally adjusted to reduce the peaks of PDN impedance.

Using the evaluation board and the capacitors in Table III, we verify the effectiveness of the proposed method by

1) PDN impedance measured at the SMA connector, and
2) radiation noise from the evaluation board by connecting an oscillator to the SMA connector.

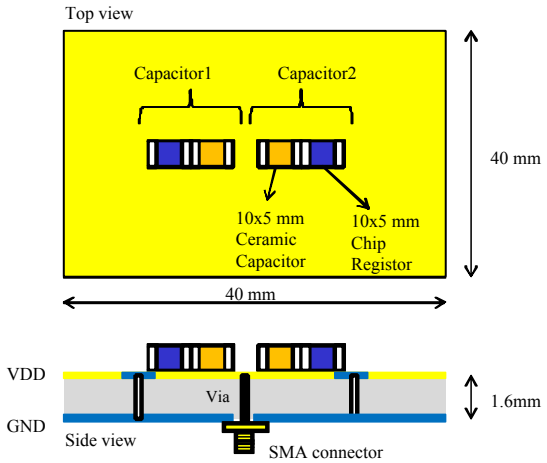

Fig. 6. Test board and instrumental setup for experiments.

TABLE III
PARAMETERS OF CAPACITORS IN EXPERIMENTS.

Condition	Capacitor 1		Capacitor 2	
	C_{c1} [μF]	R_{c1} [mΩ]	C_{c2} [F]	R_{c2} [Ω]
A	0.1	50	-	-
B	0.1	50	0.1 μ	7.5
C	0.1	50	39 p	0.05
D	0.1	50	39 p	6.8

A. Measurement results of PDN impedance

Figure 7 shows the measured impedance for different conditions in Table III. Figure 8 shows the equivalent circuit of the evaluation board, the parameters of which are determined by the measured impedance. Large ESL of the capacitors (1.6 nH) is attributed by the board thickness (1.6 mm) and the series ESL of both ceramic capacitor and SMD resistor. In Fig. 7, line A, which is the case to use one LSR capacitor, shows a peak of impedance at 600 MHz due to the parallel resonance. The resonance comes from an ESL of capacitor 1 L_{c1} and the parasitic capacitance of the plane C_p. Line B, which is the case to add an HSR capacitor that has the same capacitance value of LSR capacitor, has about 1/10 of peak impedance compared to line A. The peak impedance of line C has been slightly lower than line A, but the peak has not been eliminated. Line D, which is the proposed method, successfully reduced the peak impedance by 10x by using easy-to-fabricate capacitor parameters.

B. Measurement results of radiation noise

In order to verify the effectiveness of the proposed method in terms of radiation noise, the evaluation board has been exited by a 33 MHz pulse oscillator in a 3 m anechoic chamber. Measurement setup is shown in Fig 9. Only the result of horizontal radiation is presented in the figure because horizontal and vertical radiations have very similar trend. Here, noise peaks for condition A is represented by the envelope for easier comparison with other conditions. The figure shows that radiation noise has the peak at 600 MHz that is the same frequency as the parallel resonance of PDN impedance. This implies the cause of radiated noise comes from the parallel

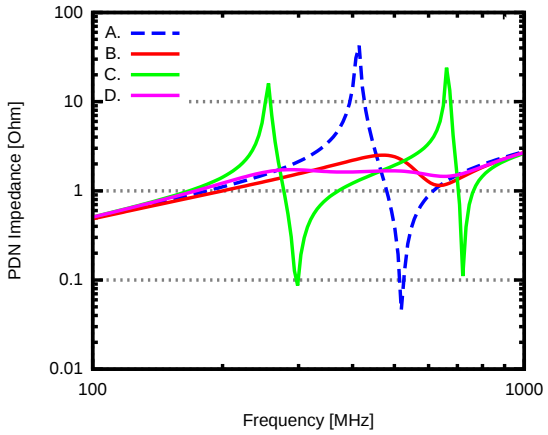

Fig. 7. Measured PDN impedance curves.

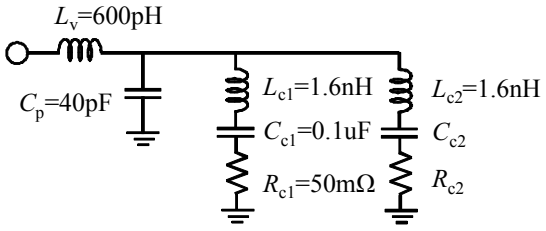

Fig. 8. Equivalent circuit model of the evaluation board.

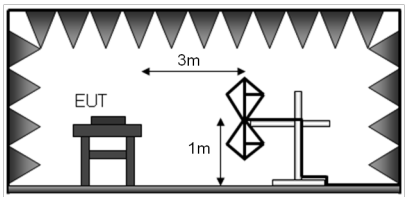

Fig. 9. Measurement conditions of radiated noise.

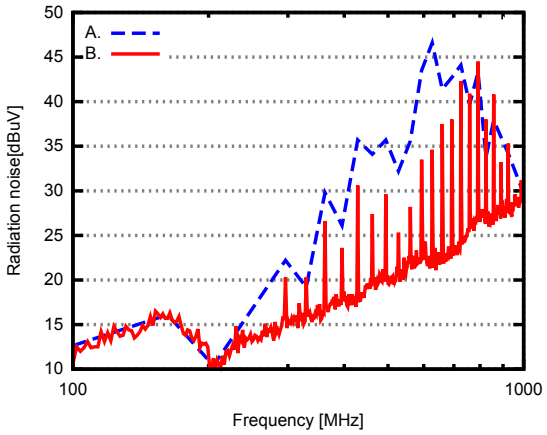

Fig. 10. Measured radiation noise of the conventional methods.

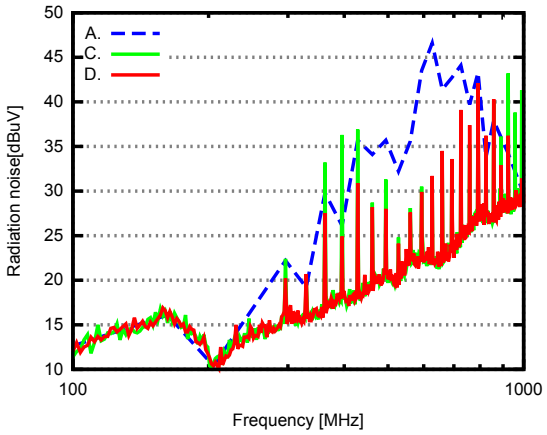

Fig. 11. Measured radiation noise of the proposed method.

resonance due to bypass capacitors. Line B shows that the conventional method reduces the radiated noise by 13 dB at 600 MHz. In the frequency range of 700 to 900 MHz, the conventional method increases the noise by 4 dB.

In Fig. 11, noise of conditions A, C and D are compared. Condition C, which uses low capacitance and LSR capacitor, has the peaks of radiation noise at 400 MHz and 900 MHz. These frequencies again equal to the parallel resonance frequencies of PDN impedance. Condition D shows that the proposed method reduces radiation noise by 15 dB. These results mean that the proposed method can equally reduce the peak impedance and radiation noise as the conventional methods without using a costly HC-HSR capacitor.

IV. Conclusion

We proposed a cost effective method to reduce the peak impedance at a parallel resonance frequency of the power distribution network. The proposed method is equally effective to the conventional method that uses an expensive HSR capacitor which has a large capacitance. Instead, the proposed method utilizes an HSR capacitor of small capacitance, which could make the fabrication cost of the capacitor inexpensive while achieving equal effectiveness with the conventional method. The effectiveness of the proposed method has been verified through test board measurements, which showed 10x suppression of PDN impedance and 15 dB suppression of radiated noise.

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