12th Optoelectronics and Communications Conference/16th International Conference on Integrated Optics and Optical Fiber Communication (OECC/IOOC2007)
Technical Digest, July 2007, Pacifico Yokohama

13P-3

Proposal for Simple Bit Timing Synchronization Technique of Mapping Optical Burst Signals for Optical Burst Switching

Ayako Iwaki, Motoharu Matsuura, Naoto Kishi, and Tetsuya Miki
Department of Information and Communication Engineering, University of Electro-Communications,
1-5-1 Chofugaoka, Chofu-shi, Tokyo 182-8585, JAPAN
Tel: +81-42-443-5218, Fax: +81-42-490-7096, Email: iwaki@ice.uec.ac.jp

Abstract

A simple bit timing synchronization technique for optical burst switching was proposed by monitoring the timing lag between optical burst signals.

1 Introduction

In future photonic networks, optical burst switching (OBS) is one of the attractive technologies due to fine bandwidth granularity and high feasibility of hardware architecture. To send control information for bandwidth allocation in OBS, two schemes have already been proposed; one is to use a channel for the control signal differing from data channel, and the other is to transmit on a channel same as data channel. Although the latter has a better channel availability for data transmission, it requires a bit timing synchronization between the control and the data signals, since both signals must be received by an optical receiver.

On the other hand, in the case of optical time division multiplexing (OTDM) systems, a number of synchronization techniques have already been proposed [1], so far. However, it is difficult to realize precise bit timing synchronization. To solve this problem, we proposed a novel bit timing synchronization technique between optical burst data.

2 Mapping burst data in optical frame

In dynamic path photonic networks [2][3], the optical burst data are mapped into an optical frame and dropped at a destination node at header information of the optical frame.

Fig. 1 show the configuration of the optical burst data mapping using an optical switch. An optical burst data from a source node is mapped into an optical frame using a 2 × 1 optical switch. The optical burst data is injected into an input port of the optical switch, while the optical frame is injected into the other port. At the same time, an electrical control signal is injected into the optical switch from the source node. The electrical control signal is employed to change passed input port of the optical switch.

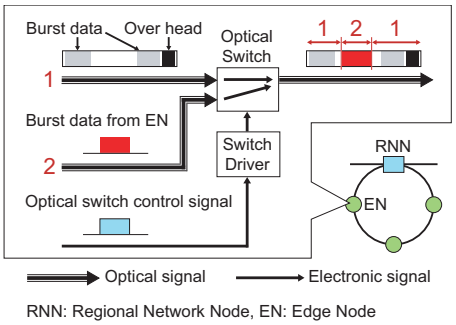

Fig. 1 Mapping burst data with optical switch

3 Bit timing synchronization

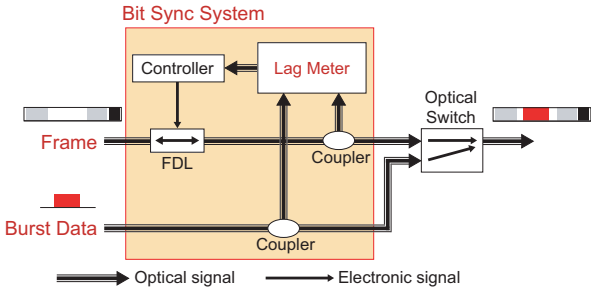

Fig. 2 Bit timing synchronization system

Fig. 2 shows configuration of the proposed bit timing synchronization system. The bit timing synchronization system consists of a timing lag meter and a tunable fiber delay line (FDL). The optical frame and burst data are launched into the lag meter, and the timing lag is detected. Using the feedback circuit based on the FDL, the timing lag can be controlled automatically.

The schematic view of the lag meter with dual-stage AND gates is depicted in Fig. 3(a). At the AND gate #1 of the timing lag meter, the part of continuous bit pattern of "010101..." in the burst signal is drawn by using the window signal as shown in Fig. 3(b). The clipped signal from the optical frame consist of a part of the padding of header, which has a continuous bit

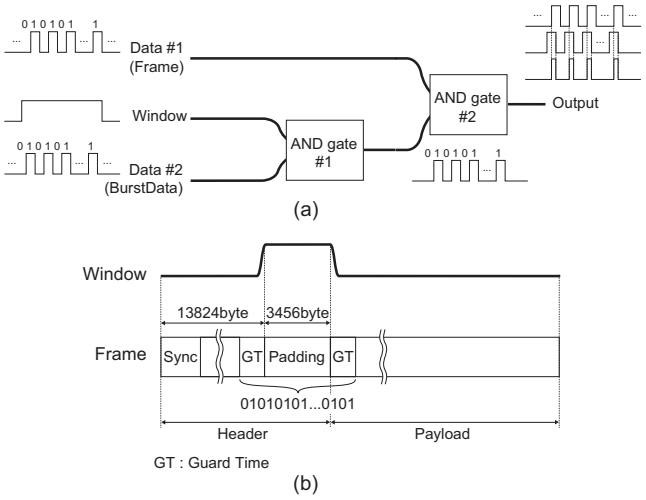

Fig. 3 Timing lag meter. (a) System configuration. (b) Coverage of window.

pattern of "010101...". The signal from the source node also has same bit pattern. Next, the frame signal and the output signal at the AND gate #1 are injected into the AND gate #2 in order to measure the overlap part of the mark bits between the frame and burst signals with each same bit pattern. Thus, the timing lag can be evaluated by the output average power at the output of the dual-stage AND gate, because the power is determined by the overlapped area of mark bits. Since high speed receiver is not needed in this scheme, we will realize a cost effective bit timing synchronization.

4 Experimental verification of the timing lag meter

To verify the availability of the proposed bit timing synchronization technique using AND gates, we demonstrated experimentally a single stage AND gate scheme by means of four-wave mixing (FWM) [4] in a semiconductor optical amplifier (SOA). Fig. 4 shows the experimental setup of the AND gate. The input lights were coupled by a 3-dB coupler and modulated by a 10 Gb/s data with the bit pattern of "010101..." using a $LiNbO_3$ modulator (LNM). The modulated lights were demultiplexed by an array waveguide grating (AWG). One of them was passed through a FDL. Erbium Doped Fiber Amplifiers (EDFAs) were employed to compensate the insertion loss of 3-dB coupler, LNM and AWG. After that, the signals were coupled by 3-dB coupler and injected into a SOA. In the SOA, the overlapped light component between two lights was generated by FWM, and only passed through the AWG. At the output of the AWG, the average output power was monitored by an optical power meter. In this experiment, the wavelength of input lights were 1555.98 nm and 1556.79 nm, and their input powers into the SOA were 8 dBm and 5 dBm, respectively.

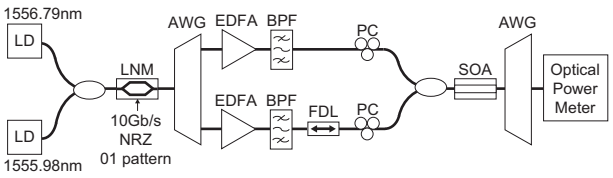

Fig. 4 Experimental setup of the AND gate #2

Fig. 5 shows the measured output average power with changing the time delay of the FDL. It can be clearly seen that the output power was changed periodically, and the period corresponded to the 2 bit time of the 10 Gb/s data, '0' and '1'.

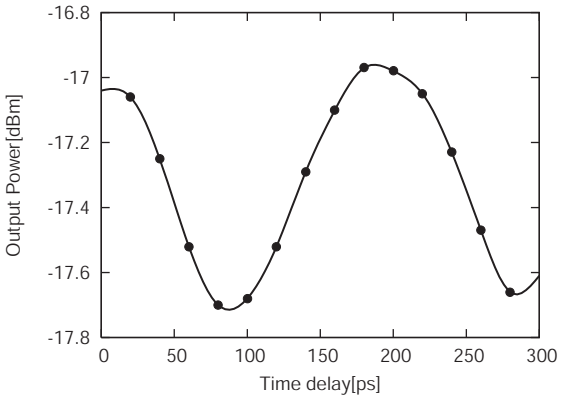

Fig. 5 Delay by FDL vs. output average power

This indicates that the timing lag can be detected by the output average power. Therefore, the timing lag will be controlled automatically, if the time delay of the FDL is adjusted by monitoring the change of the output power.

5 Conclusion

We proposed a bit timing synchronization system for optical burst switching by measuring the timing lag between two optical signals. We also verified the operation using a prototype of the timing lag meter.

References

[1] For example, S.Ohteru et al., IEEE PTL, Vol. 8, pp. 1181-1183, 1996.

[2] L.R.Nunes et al., IEICE Trans. Commun., vol. E86-B, no. 3, pp. 1031-1039, 2003.

[3] T.Miki et al., in Proc. OECC2006, 5E4-2, 2006.

[4] C.Yu et al., IEEE PTL., Vol. 17, pp. 636-638, 2005.