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# Block Turbo Code Encoded 24.8 Gbps RZ-DQPSK Experiment using Parallel Prefix Network based Differential Precoder

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**We experimentally demonstrate true FEC-encoded PRBS transmission at 20 Gbps using a live precoder for return-to-zero differential quadrature phase-shift keying, together with a block turbo code forward error correction with soft-decoding.**

## 1. Introduction

Modulation formats have been a major concern for the high speed optical transmission systems that are expected to exhibit a larger transmission capacity through higher spectral efficiencies [1]. Return-to-zero differential quadrature phase-shift keying (RZ-DQPSK) is a promising format owing to its high spectral efficiency, larger tolerance to chromatic dispersion and polarization-mode-dispersion as compared to RZ-DPSK. On the other hand, forward error correction (FEC) is also indispensable for improving received BER performance. Recently, we have developed above two technologies, *i.e.* RZ-DQPSK [2] and block turbo code (BTC) FEC [3]. However, to date each technology challenge has been pursued independently, and no experimental demonstration has yet been reported of these in a true combination.

In this paper, we demonstrate actual BTC FEC encoded RZ-DQPSK transmission at 24.8 Gbps using a live evaluation circuit. Very large scale LSI technology and a novel differential precoder [4] make implementation of this combination possible.

## 2. Block Turbo Code FEC encoded DQPSK

DQPSK requires a differential precoder circuit to map the input information onto four phase states. A well-known serial differential precoder consists of a flip-flop with a feedback path. However, when the symbol rate exceeds 10 Gsymbols/s, propagation delay caused by the feedback path creates a bottleneck in a circuit implemented in currently available high-speed semiconductor technology, *e.g.* SiGe HBT. Therefore, most transmission experiments reported to date used either pre-calculated pseudo random binary sequence (PRBS) patterns or programmed data received without precoding. We designed a novel parallelized precoder for DQPSK with a parallel prefix network, which is the well known computer engineers' adder circuit. The proposed precoder makes it possible simultaneously to reduce the circuit size at a rate of $k\log_2 k$, and the required speed at a rate of $(s\log_2 k)/k$ [4], where $k$ is the parallel expansion number and $s$ is the symbol rate. It allows for an implementation by standard CMOS process.

Concatenated codes based on hard decision and iterative decoding are widely used in submarine line terminals. One of the best performing second generation FECs shows an NCG of 9.4 dB with a redundancy of 25%. That appears in ITU-T G.975.1 as two orthogonally interleaved BCH codes. We have developed a superior FEC LSI using BTC with 3-bit soft decision that outperforms every existing FEC LSI. The codeword is based on a BCH(144,128) x BCH(256,239) product code having a minimum distance of 30. The bit rate for STM-64 is 12.4 Gb/s with a redundancy of 23.6%. The 0.13 μm CMOS technology enabled full integration into a circuit volume of approximately 16 M gates. The soft decision IC was manufactured in 0.2 μm SiGe BiCMOS with $f_t$ = 120 GHz. Approximately 20,000 bipolar and 1,500 CMOS transistors were placed on the 9 x 9 mm chip.

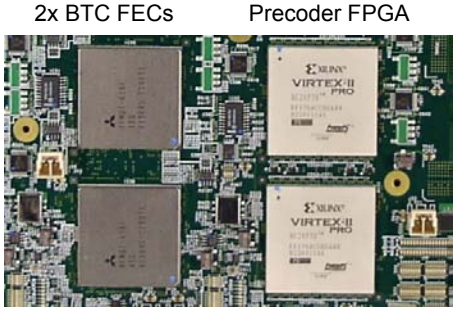


Fig. 1 FECs and Precoder onto the circuit board

The LSIs show an NCG of 10.1 dB at 12.4 Gb/s and provide a SONET/SDH compliant section and line processing for OC-192/STM-64. The input client signal is mapped in two ways. The G.709 FEC in the incoming OTN signal is decoded first, then the OTU2 overhead is extracted. In the case of an STM-64 client signal, the overhead is terminated and its performance is monitored. The client signal is then mapped on to the BTC framer with an OPU2/ODU2/OTU2v overhead. The encoded 12.4 Gb/s signal is output to the line side. At the receiver side, three 12.4 Gb/s signals, *i.e.* the hard decision information and the MSB and LSB confidence information from the soft decision IC, are decoded by the BTC decoder. The OTU2v/ODU2/OPU2 overhead is terminated and demapped by the BTC de-framer. The OTN overhead is generated before launching to the client side.

### 3. Experiment and discussion

We built the BTC FEC LSI and the parallel prefix precoder onto a live circuit board. The precoder was implemented in a commercially available FPGA, operating at only 97 Mb/s, with a parallel expansion *k* of 128. The circuit board, shown in Fig.1, was designed for a 24.8 Gb/s (=12.4 Gsymbols/s) RZ-DQPSK system.

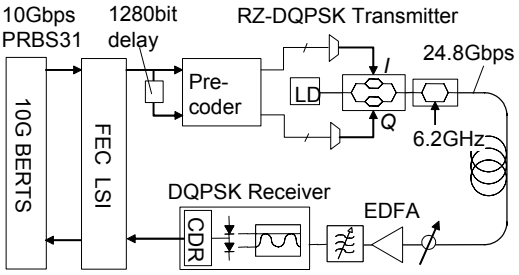


Fig.2 Experimental setup for BTC FEC encoded 20 Gb/s RZ-DQPSK using proposed precoder.

Fig. 2 illustrates the experimental setup for true FEC encoded/decoded 20 Gb/s PRBS transmission. A PRBS31 at 10 Gb/s was FEC-encoded by the block turbo code LSI with FEC redundancy of 23.6%, then split and electrically decorrelated by the 1280 bit delay circuit in order to generate two independent tributaries. Each tributary was differentially precoded by the precoder, serialized by the 128:1 electrical MUX, then converted to 24.8 Gb/s RZ-DQPSK optical signals by a parallel Mach-Zehnder I/Q modulator followed by a pulse-carving AM modulator. The I/Q modulator was biased at its null points and driven with a peak-to-peak voltage of $2V\pi$ by the precoded data streams. After some meters of single-mode fiber transmission, the optically preamplified RZ-DQPSK signal was input into a Mach-Zehnder delay interferometer (MZDI) followed by a balanced photo-detector. One of the tributaries was selected by adjusting the phase of the MZDI. A clear eye opening was observed. The received signal was FEC-decoded by the FEC LSI. The BER of the decoded data was measured at 10 Gb/s.

The error correction performance was tested by changing the received power. The result is plotted in Fig. 3. Worse BER was successfully improved by BTC FEC. An output BER of better than $3x10^{-12}$ was obtained when a received power of -42.3dBm. Taking the 23.6% bit rate increase into consideration, the net coding gain was 10.1 dB at the post-FEC BER of $10^{-13}$. This is fully the same error correction capability that was measured previously for RZ-OOK [3]. Narrow spectrum of RZ-DQPSK was observed as an inset of Fig. 3.

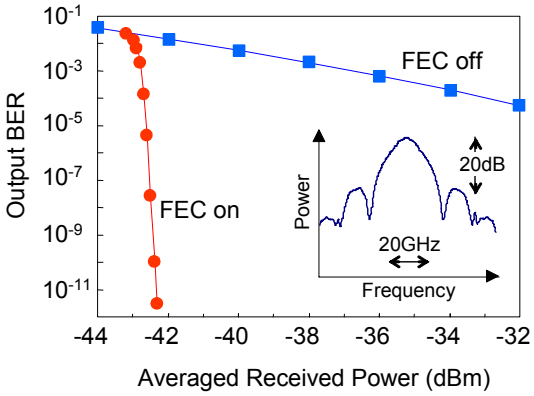


Fig.3 Measured BER performance for 24.8 Gbps RZ-DQPSK with BTC FEC

### 4. Conclusion

We have demonstrated two promising technologies, i.e. RZ-DQPSK with the differential precoder and block turbo code FEC. We showed experimentally the BER performance of the combination of RZ-DQPSK and BTC FEC. These two technologies will together open up new possibilities for robust capacity deployment in the very high speed transmission systems.

### References


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[4] Y. Konishi *et al.*, OFC/NFOEC2006, OThR3, March 2006.