A Study of Common Mode Noise Current of Bridgeless PFC Circuit Considering Voltage Change in Y-Capacitors

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***Abstract*— Since the loss of input rectifying diode bridge in the conventional PFC circuit reduces the efficiency, the bridgeless PFC circuit has been proposed. However, the performances of EMC in some bridgeless PFC circuits are unsatisfactory. In order to improve noise performance, the noise mechanism should be investigated as the first step. In this study, common mode noise current of conventional bridge PFC circuit and totem-pole bridgeless PFC circuit have been analyzed considering the voltage change in Y-capacitors. Additionally a method has been proposed to suppress common mode noise current by about 40dB on the totem-pole bridgeless PFC circuit.**

Keywords—Bridgeless PFC circuit, Totem-pole type, Common mode noise current, Y-capacitor

I. INTRODUCTION

Because of the its control strategy and brief structure, the conventional bridge PFC circuit has been widely used in various applications. However, the loss of input rectifying diode bridge cannot be ignored as the switch frequency of the switching power supply is efficiently designed. To improve the efficiency of PFC circuits, bridgeless PFC circuits have been proposed. The two most representative ones are shown in Fig. 1 and Fig. 3.

In the first circuit (Fig.1. asymmetric one), during the negative half circle of input voltage, the operation of switch S_2 brings acute change of voltage across the parasitic capacitor frequently leading to the occurrence of huge common mode conductional noise. In order to suppress the noise the semi bridgeless PFC circuit shown in Fig. 2 was proposed.

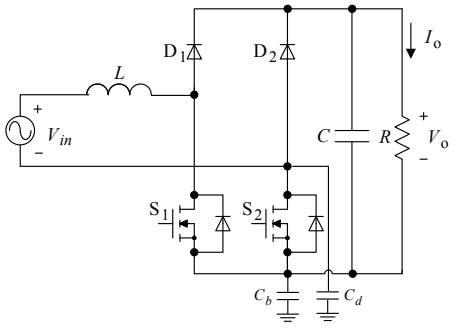

Fig. 1. Asymmetric inductor type bridgeless PFC circuit

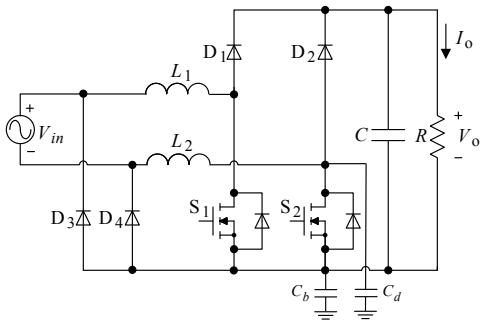

Fig. 2. Semi bridgeless PFC circuit

By adding the symmetrical inductor L_2, clamp diode D_3 and D_4, the voltage across the parasitic capacitors (C_b and C_d) can be kept constant.

In the second circuit (Fig.3. totem-pole one), two severe problems restricts its application.

The 1st one: the recovery speed of body diode in general-purpose MOSFET is so slow that makes S_1 and S_2 conduct in the same time leading to the destruction of the circuits. Therefore, the MOSFET with fast recovery speed should be used in totem-pole topology. Additionally, the use of fast recovery diode instead of MOSFET is another option but the topology should be changed to the one shown in the Fig. 7 which will be focused to discuss the mechanism of common mode noise since the way common mode noise occurs is same compared with the conventional totem-pole one.

The 2nd one: the noise performance of totem-pole bridgeless PFC circuit is unsatisfactory compared with conventional bridge PFC circuit shown in Fig. 4 and Fig. 5. In order to improve the noise performance, the noise mechanism should be investigated as the first step.

In the application of switching power supply, the Y-capacitors is usually used in the input bus of the PFC circuit to suppress the common mode noise produced by the power source. However, in some topologies, the Y-capacitors might act as a noise source also. Therefore it is worth to pay attention to Y-capacitors. In this study, the common mode noise current of conventional bridge PFC circuit and totem-pole bridgeless PFC circuit was investigated taking into

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consideration the voltage change in Y-capacitors. We propose a method for suppressing common mode noise. The experiment was to verify the accuracy of the proposed method.

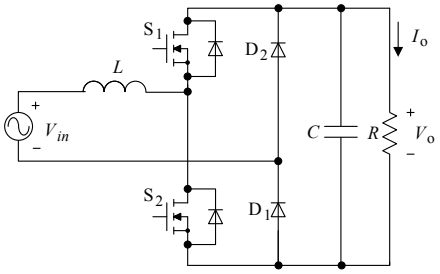

Fig. 3. Totem-pole bridgeless PFC circuit

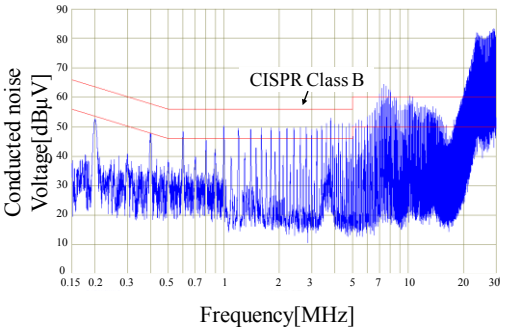

Fig. 4. Conductional common mode noise of conventional bridge PFC circuit

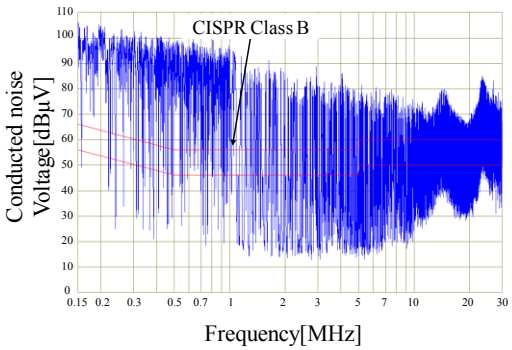

Fig. 5. Conductional common mode noise of totem-pole PFC circuit

II. Noise Analysis of Various PFC Circuits

In this study, two PFC circuits shown in Fig.6 and Fig.7 were used to analyze the voltage V_{fg} and current I_{fg} (fg: frame ground) of capacitor C_{fg}.

①Circuit A (Conventional Bridge Type) (Fig. 6): In the positive half cycle of the input voltage, as diode D_4 stays on, $V_{fg} = V_{cy2}$. Additionally in the negative half cycle, equation $V_{fg} = V_{cy1}$ can be obtained similarly. Since change in V_{cy1} and V_{cy2} are very slow, these could be considered as constant values during a certain temporary time. At the zero crossing of the input voltage, both V_{cy1} and V_{cy2} equal zero, which indicates that no step change of V_{fg} occurs during the entire period. Therefore, no spike current I_{fg} flows all the time.

②Circuit B (Totem Pole Bridgeless Type) (Fig. 7): During the positive half cycle, diode D_4 stays on, so that $V_{fg} = V_{cy2}$. However, when the polarity of the input voltage changes, D_3 turns ON whenever D_4 turns OFF, as shown in Fig. 7, the expression of V_{fg} changes to $V_{fg} = V_{cy2} + V_o$. Therefore step change of voltage occurs here, leading to the occurrence of spike current I_{fg}.

In conclusion, by observing the variation of voltage across capacitor C_{fg}, the value and duration of the common mode noise current could be investigated easily.

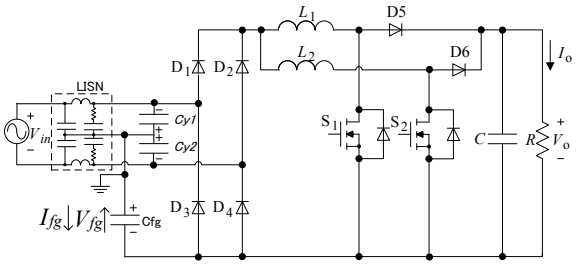

Fig. 6. Conventional bridge PFC circuit

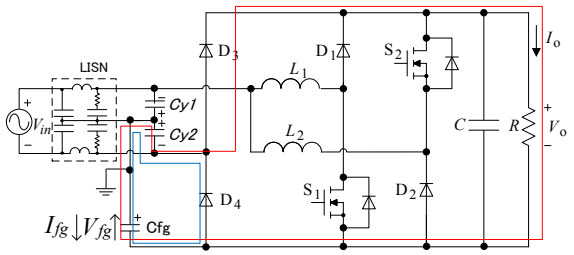

Fig. 7. Totem-pole bridgeless PFC circuit with fast recovery diode

III. Noise Analysis of the Totem-Pole Bridgeless PFC Circuit at Zero Crossing

We demonstrated that the common mode noise current occurs only when the polarity of input voltage changes.

Because the topology of totem-pole bridgeless PFC circuit is symmetrical, we analyzed only the commutation process at the zero crossing when V_{in} transforms from negative to positive. The equivalent circuit is shown in Fig. 8. The Y connection of capacitors C_{fg}, C_{y1}, and C_{y2} is transformed to △ connection as showed in Fig. 9.

When switch S_1 turns on, because the capacitor C_{yc} ($C_{yc} = C_1 + C_2$) has not been discharged yet, the energy stored will be added to inductor L_1 directly. Spike current I_{fg} flows through the path shown in Fig. 10. Additionally it can be described by equation (1). The voltage of C_{yc} can be described by equation (2) in the same way.

$$I_{fg} = I_{L_1} = \sqrt{\frac{C_{yc}}{L_1}} V_o \sin \frac{1}{\sqrt{L_1 \cdot C_{yc}}} t \quad (1)$$

$$V_{C_{yc}} = V_o \cos \frac{1}{\sqrt{L_1 \cdot C_{yc}}} t \quad (2)$$

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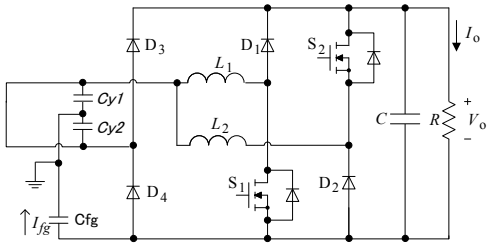

Fig. 8. Equivalent circuit (V_{in}=0)

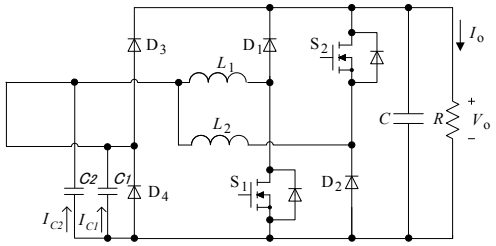

Fig. 9. △Connection equivalent circuit

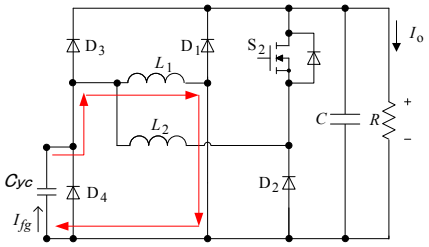

Fig. 10. Noise current path (switch S_1 ON)

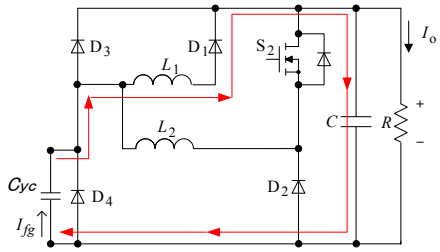

Fig. 11. Noise current path (switch S_1 OFF)

For example, when values of the elements are designed as L_1=200 μH, C_{y1}=C_{y2}=2 nF, V_{fg}=1 nF, V_o=390 V, discharge time of C_{yc} is calculated by equation $0.5\pi\sqrt{L_1 \cdot C_{yc}} = 0.6\mu s$. If switch S_1 stays ON for a sufficient time at the 1st switch cycle, the energy stored in C_{yc} could be released to L_1 thoroughly. Additionally the peak value of spike current I_{fg} can also be calculated as $V_o\sqrt{C_{yc}/L_1} \approx 1A$. However, many parasitic capacitors should be considered so that the discharge time is longer than 0.6μs and the peak value is larger than 1A. It means that during the 1st switch cycle, there is not sufficient time for C_{yc} to be discharged completely. The spike current flows through paths shown in Fig. 10 and Fig. 11 repeatedly. Therefore, the equation which describes the peak value of spike current should be adjusted to $n \cdot V_o\sqrt{C_{yc}/L_1}$, (n>1). Additionally, the discharge time should be adjusted to $m \cdot 0.5\pi\sqrt{L_1 \cdot C_{yc}}$, (m>1). The coefficient m and n determined by the control strategy has not been discussed in detail here.

The above analysis indicates, that C_{yc} and L_1 could affect the value and duration of spike current I_{fg}.

IV. Proposed Method of Noise Suppression for Totem Pole Bridgeless PFC Circuit

Add capacitor C_4 in parallel with D_4 as shown in Fig. 12. Equations (1) and (2) should be rewritten as follows:

$$I_{L_1} = \sqrt{\frac{C_{yc}+C_4}{L_1}} V_o \sin\frac{1}{\sqrt{L_1(C_{yc}+C_4)}}t \quad (3)$$

$$I_{fg} = \frac{C_{yc}}{C_{yc}+C_4} I_{L_1} = \frac{C_{yc}}{\sqrt{L_1(C_{yc}+C_4)}} V_o \sin\frac{1}{\sqrt{L_1(C_{yc}+C_4)}}t \quad (4)$$

$$V_{C_{yc}} = V_o \cos\frac{1}{\sqrt{L_1(C_{yc}+C_4)}}t \quad (5)$$

Unlike what has been indicated that common mode noise becomes larger if C_4 is added in parallel with D_4 [1], this method is effective. From the equations (4) and (3), by adding capacitor C_4, I_{fg} becomes smaller, although the current flow through L_1 becomes larger. It means that the common mode noise current flowing through capacitor C_{yc} is suppressed. Fig. 13 shows the spike current path (S_1 ON: red; S_1 OFF: red + blue), since $C_4 >> C_{yc}$, the current I_{fg} is very small. The experimental results are shown in Fig. 14, 15 and 16. From Fig. 14 and Fig. 15, it is clear that current I_{fg} is suppressed efficiently, and from Fig. 16, it is evident that the common mode noise can be reduced by approximately 40 dB only by adding C_4 in parallel with D_4, hence, it verifies the accuracy of the proposed method. Furthermore, the efficiency is almost the same as that of the conventional one.

By increasing the capacitance of C_4 the common mode noise could be suppressed more efficiently. However, owing to the resonation between L_1 (or L_2) and C_4, the resonant current flowing through the input inductors every time when the polarity of input current changes will become bigger. Therefore the value of C_4 should not be too large.

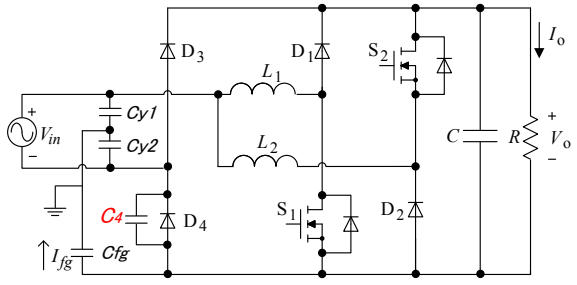

Fig. 12. Circuit with capacitor C_4 added

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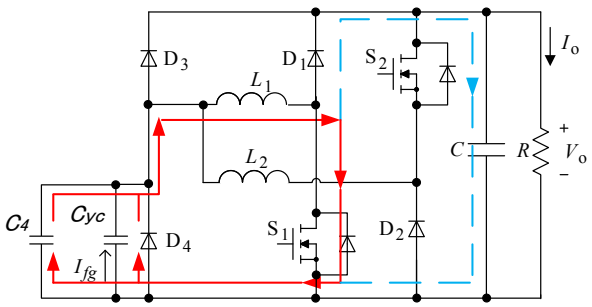

Fig. 13. Noise current path with capacitor C_4 added

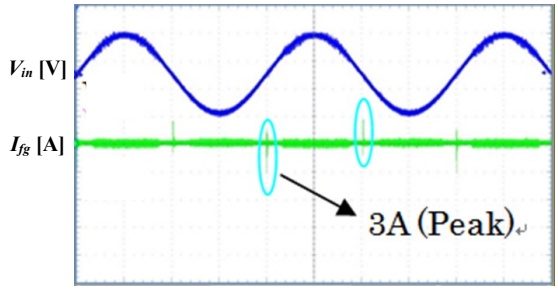

Fig. 14. Common mode noise current I_{fg} without capacitor C_4

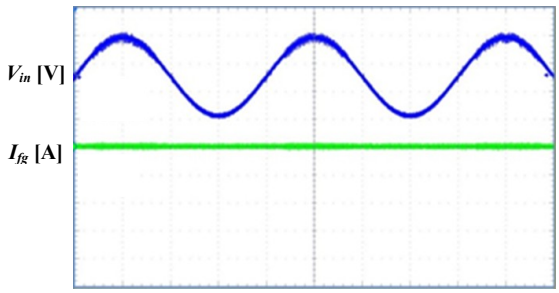

Fig. 15. Common mode noise current I_{fg} with capacitor C_4=500nF

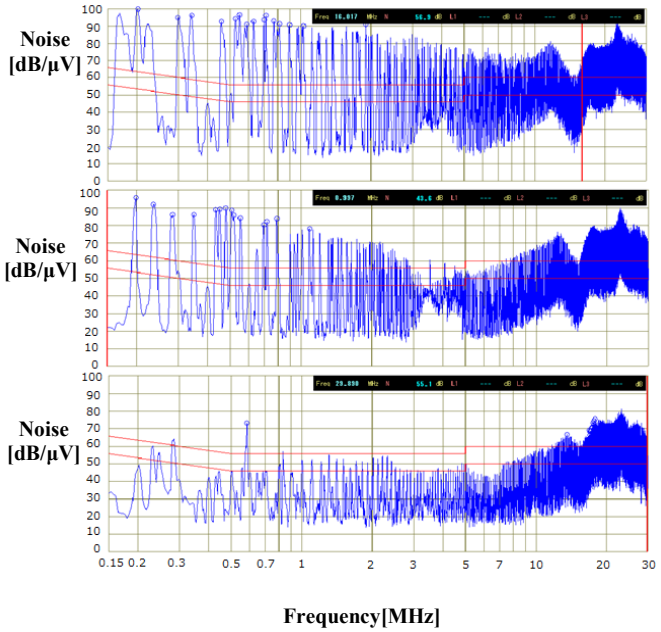

Fig.16. Conductional common mode noise in the cases of without C_4, with C_4=100 nF and with C_4=500 nF (from up to down)

V. Conclusion

This paper presents the method how to predict the common mode noise current on PFC circuits taking into consideration the voltage change in Y-capacitors.

We demonstrated that common mode noise current occurs only at zero crossing of the input voltage on the totem-pole bridgeless PFC circuit. Furthermore, we proposed a method to suppress the common mode noise current, and verified the accuracy by experiments. By using the proposed method, the conductional common mode noise could be reduced by approximately 40 dB.

The common mode noise might be reduced even more by increasing the capacitance of C_4, however the resonant current flowing through inductor L_1 also becomes larger. The tradeoff between common mode noise and resonant current flowing through the input inductors should be considered carefully when selecting the capacitance of C_4.

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