Software-related EMI Model Reduction for Two-stage Pipeline Microcontroller

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***Abstract*—This paper proposes a software-related conducted electromagnetic interference (SW-cEMI) model reduction process for two-stage pipelined microcontroller (μC). This paper is based on a black-box transfer function (BBTF) cEMI model building technology and a new proposed decomposition method to reduce the BBTF model (rBBTF) to a reasonable model size. If the number of a μC's machine codes is *N* and the pipeline stage is *p*, the BBTF model size would be $2N^p$. The rBBTF method can reduce the size to *2Np*. By the propose method, the simulation and estimation of the target μC's SW-cEMI behaviors become efficient without sacrificing much accuracy. Both of the measurement and simulation results are given to justify the proposed modeling method.**

Keywords—recuced black-box transfer function conducted EMI modeling; software-level cEMI modeling; pipelined microcontroller EMI modeling

I. INTRODUCTION

Digital IC is driven by clock. The conducted electromagnetic interference (cEMI) of a digital system is generally induced by clock signals. Although the clock-induced noise is the main source for digital systems' cEMI, it is a subtle problem that the cEMI do NOT depend solely on clock.

There are many factors affecting software-related cEMI (SW-cEMI) [1] during software execution in a μC. simultaneously switching noise (SSN) and transient current can be controlled by many μC's features, for example, output driving-capacity, PLL for different power modes, jitter, clock-gating..

Fig. 1 is a time domain power fluctuation measurement result of 8051 microcontroller (μC) from our laboratory. The blue and green lines represents different machine codes' (add and mov) measurements according to IEC 61967-4 [2].

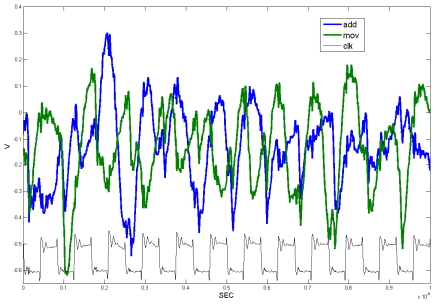

Fig. 1 Power fluctuations of a 8051system with different machine codes during execution

Fig. 1 clearly shows that different machine codes have different cEMI behaviors. Some efforts are proposed in [4][5]. These efforts require some preliminary assumptions, such as, a close-form or a fixed RLC network approximation for IC PDN is good enough for cEMI estimation, the RESET condition is similar to normal execution cEMI and can be used as a reference to the other execution condition, the internal impedance of a target μC remains the same when it executes at different conditions or different machine codes, or the SW-cEMI effect is very weak and can be neglected.

A universal SW-cEMI model building technique called black-box impulse response (BBIR) modeling method [6] is proposed for such model building process without any of the assumptions above. An estimation and measurement justified the BBIR method is necessary, efficient and effective below 100MHz. This method can estimate both the IC's internal power distribution network impedance (IntZ) and internal current activity (IntCA) at the same time, frequency point by frequency point.

Modern μC uses pipeline stages [7] for efficient execution. Many advantages, techniques, and modifications of the pipelined design can be founded in [8]. Despite of the advantages, pipelined designs bring many research issues, such as, execution ordering optimization and estimation, the compiler optimization, power estimation and, thus, the SW-cEMI model building. Because the execution in a μC is no longer related to single machine code, the cEMI model and the power model of μC are much more complex than ever.

Due to the reasons above, SW-cEMI modeling is far from a simple data collection tasks based from the measurement of IEC-61967-4 [2] standards. This paper tries to propose a solution to such issue based on BBIR and apply it onto a 2-stage pipeline μC to build SW-cEMI model. Since BBIR is so modified in this paper that it is no longer a black-box 'impulse response' model and the characteristics are fundamentally based on Laplace-domain transfer function, the proposed μC SW-cEMI modeling method is extended and called a black-box transfer function (BBTF) model in the following paper.

This method can be extended to other 2-stage pipeline μCs. With a little more modification, we hope that it can be suited for 3/4/5-stage pipeline μC in the future.

II. SOFTWARE-RELATED CEMI MODEL: INTZ AND INTCA REDUCTION BY RBBTF METHOD

2.1 Previous cEMI model

ICEM [9] is the standard of IC-EMC modeling method

which is used to predict conducted and radiated electromagnetic interference of microcontroller. This model has two major parts: the Power Distribution Network (PDN) and initiative current source (IA). PDN filters and carries the transient responses of the current source in the model to the PCB.

2.2 ICM, IntZ/IntCA set of SW-cEMI, and ICM database

In [6], the estimated PDNs when executing different machine code can be analyzed individually and grouped into a set. The set is called the "IC's internal impedance set" (IntZ set).

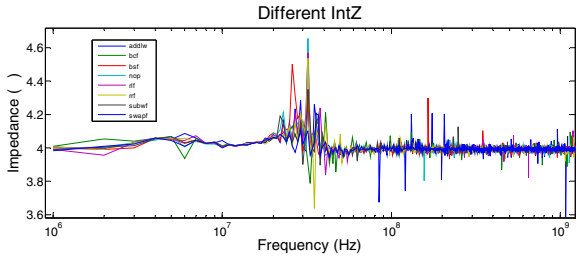

Fig. 2 Estimated internal impedances of different machine codes of a μC (adapted from [6])

We modify the ICEM to a SW-cEMI model called the Machine code Current Model (ICM) [1] which can estimate the SW-cEMI behavior of target μCs. Different from the original ICEM, ICM's current source is subdivided into different current sources related to each machine code of the target μC. All of these current sources are grouped into a set. We call it as the "IC's internal current activity set" (IntCA set).

These two sets are the ICM's kernel information. Any simulations and estimations through ICM depend heavily on these two sets. We call the IntCA/IntZ set the "ICM database."

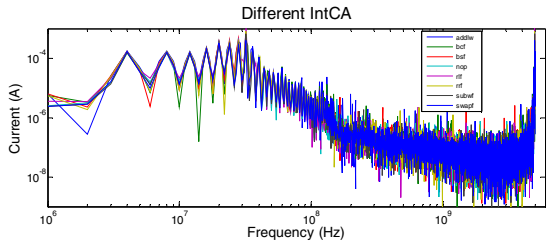

Fig. 3 Estimated internal current activities of different machine codes of a μC (adapted from [6])

BBTF modeling method abstracts IntZ/IntCA as an Laplace transfer function. It tries to measure PCB responses and estimate the transfer functions of IntCA and IntZ.

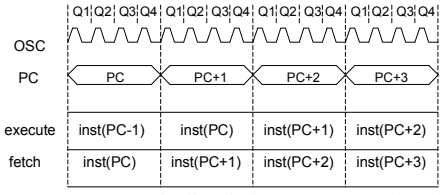

Fig. 4 PIC12F629's 2 stage pipeline timing sequence (adapted from [PIC])

2.3 SW-cEMI model for pipelined μC and rBBTF method

The target μC is PIC12F629. This μC contains two pipeline stages (Fig. 4) which are called "fetch stage" and "execution stage." This means that IntZ/IntCA modeled by BBTF involves 2 machine codes in different stages of the μC.

Fig. 5 shows the power fluctuations of the same two machine codes but with different execution orders. It is easy to see that the power fluctuations of these two sequences are different. This means that the SW-cEMI behaviors are sensitive to the order of the machine codes.

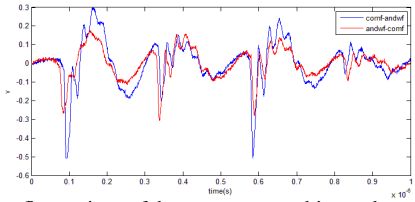

Fig. 5 Power fluctuations of the same two machine codes with different execution sequence

Generally, if a μC has N machine codes, the number of pipeline stages is p, and the number of frequency responses to be measured is k, the IntZ/IntCA size is kN^p. In our μC case, assuming each element in IntCA set has 5000 frequencies to represent the measurements (Fig. 2 and Fig. 3 is a single element of IntZ and IntCA set). The size of the set requires $5000 \times 2 \times (N^p)$ floating points (5000 complex numbers = 5000×2 floating points). In our case, the size is 23,040,000 floating points ($N=48$, $p=2$) for IntCA and IntZ set size.

For nowadays computer capacity, it is not so large comparing to the large storage size of current hard drive. However, larger size of IntZ/IntCA set can make the simulation slower. Another issue is that, for industry applications, general μC's N and p values are not so small ($N=100\sim400$, $p=1\sim5$, for the most popular industrial μC products). The IntZ/IntCA set size would be enormously large for these μC (about 10^2-10^{17} floating points). Some of the sizes exceed even the most powerful computer's storage, index, or access capability. This paper proposes a way to reduce the size of the ICM database. The process can reduce simulation and estimation time.

III. The Proposed rBBTF Methods for IntZ/IntCA Set Reduction

Here, we use 3 machine codes in a 2-stage pipeline μC as an example for the IntZ/IntCA set size reduction ($N=3$, $p=2$) demonstration. This method can reduce the set size from N^p to Np. This will reduce the size of IntZ set from 9 to 6 and so is the IntCA set size.

We denote the three machine codes as A, B, and C. And we denote these 3 machine codes in different pipeline stages as:

$$\begin{cases} \text{Af, Bf, Cf} & \text{, if it is in execute (front) stage} \\ \text{Ae, Be, Ce} & \text{, if it is in fetch (end) stage} \end{cases}$$,where the "front" means the stage is nearer to the output of the μC and "end" means farer.

There are 9 combinations (elements) in IntCA and IntZ set each. Each combination (Fig. 2 or Fig. 3 as examples) has 5000 frequency points (responses).

We separate the SW-cEMI effect of these machine codes of different stages below:

$$Ax_f = r_f$$

Where A is defined as the pipeline-associated matrix, $x(f)$ is the frequency response to be reduced, and the $r(f)$ is the frequency responses derived from BBTF method.

The pipeline-associated matrix (A) contains only 0/1 which indicates the combination of machine codes involved:

$$\overbrace{\begin{bmatrix} A_e & A_f & B_e & B_f & C_e & C_f \\ 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 \end{bmatrix}_{9\times 6}}^{A}$$

,where the entry of the matrix =

$$\begin{cases} 1 & \text{, If the corresponding frequence response decuded from BBTF } (r_f) \text{ involves in this machine code} \\ 0 & \text{, otherwise} \end{cases}$$

The frequency responses to be reduced ($x(f)$) and the frequency responses from BBTF ($r(f)$) are shown in the following.

$$\overbrace{\begin{bmatrix} A_e \\ A_f \\ B_e \\ B_f \\ C_e \\ C_f \end{bmatrix}_{6\times 1}}^{x_f} , \quad \overbrace{\begin{bmatrix} r_1 \\ r_2 \\ r_3 \\ r_4 \\ r_5 \\ r_6 \end{bmatrix}_{6\times 1}}^{r_f}$$

The equation above can be solved by inverse of A if it is square and invertible. Unfortunately, it is not. This problem can be solved by linear algebra that the projection from higher dimensions to lower dimensions:

$$Ax=Y \quad \rightarrow \quad x=A^{-1}Y \qquad \text{(not possible in this case)}$$
$$Ax=Y \quad \rightarrow \quad A^TAx = A^TY$$
$$\rightarrow x = (A^TA)^{-1}A^TY \equiv pinv(A)Y \qquad \text{(solvable)}$$

The technique above solves one equation for one single frequency. All the x_f and r_f elements are complex numbers and only for single frequency. Other frequencies can be solved by the same skill. Fig. 6 shows the concepts. Thus, the equations in this example have 5000 x_f matrix variables to be solved and 5000 r_f matrixes for different frequencies (Fig. 6).

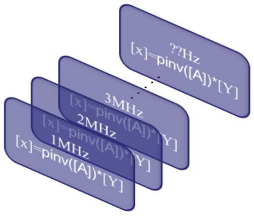

Fig. 6 The frequency response reduction calculation for all frequencies.

IV. Simulation and Measurement Result

4.1 Environment setups

The DUT to be estimated is a commercial µC PIC12F629. The operation frequency is 4MHz. The proposed rBBTF method must be given a deduced IntZ/IntCA set by BBTF to start the reduction process. The BBTF method can measure and deduce IntZ/IntCA set without any prior knowledge of the µC's internal information. We estimate the µC's IntZ/IntCA set by two PCB boards.

The PCB1, PCB2, and PCBv are specially designed 3 PCB boards with the same µC that their board-level impedance (Z_{PCB}) are NOT the same. The Z_{PCB} of PCB1 and PCB2 are not following the IEC 61967 standards. Z_{PCB} of PCBv is designed according to the standard. TABLE I shows the Z_{PCB} of the each board. The oscilloscope is DPO72004 (Fig. 7).

TABLE I. Testing board Z_{PCB}

	Z_{PCB}
PCB1	1//(s×470e-6)
PCB2	1000+1/(s×6.8e-9)
PCBv	51+1/(s×6.8e-9)

Fig. 7 Testing setups

4.2 Accuracy of the proposed method

Fig. 8 shows the original PCB1 and PCB2 time domain SW-cEMI measurement running the same machine code sequence. The PCBv's SW-cEMI can be estimated when running the same machine code sequence (Fig. 9 blue line).

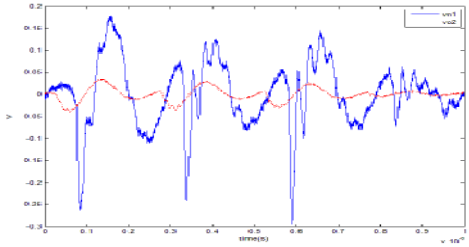

Fig. 8 Machine cycle Vo of PCB1 and PCB2

After the IntZ/IntCA set are deduced by BBTF method, the proposed rBBTF method can be used to reduce them. The final measurement of PCBv is shown in Fig. 9. The estimation deduced from PCB1 and PCB2 by BBTF and rBBTF are also shown in Fig. 9.

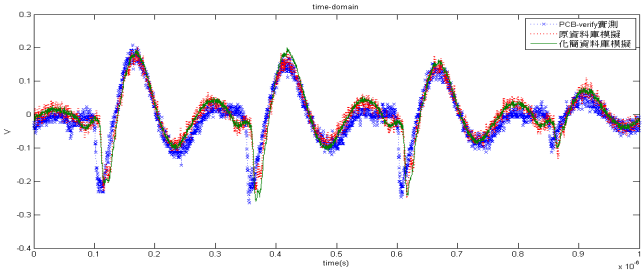

Fig. 9 Time domain cEMI of PCBv for one machine code: measurement, estimation of by BBTF, and estimation by new proposed rBBTF.

In Fig. 9, blue line is the measurement result, red line is the estimation from BBTF method, and the green line is the rBBTF method. It shows the time domain estimation is very accurate. Fig. 10 shows the frequency domain estimations which are also very accuracy within 100MHz for amplitude and 10MHz for phase.

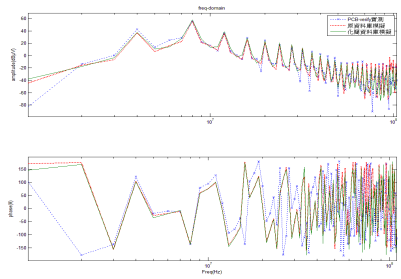

Fig. 10 Frequency domain cEMI accuracy of PCBv for one machine code: measurement, BBTF estimation, and rBBTF estimation.

4.3 Size reduction

For PIC μC (*N=48, p=2*), the total size reductions of IntZ/IntCA sets are shown in TABLE II. From Fig. 9, Fig. 10, and TABLE II, about 91.6% data are reduced without sacrificing much estimation accuracy.

TABLE II. Size reduction

	BBTF	rBBTF	Reduction ratio
IntZ	31.4 MB	2.62 MB	8.34%
IntCA	32.5 MB	2.71 MB	8.34%

4.4 Speedups

The new proposed rBBTF method needs time in the IntCA/IntZ set size reduction while the original BBTF do not. The reduction time takes about 120 sec. However, during the estimation phase, the new proposed rBBTF method takes less simulation time (Fig. 11). Fig. 11 shows a log-log plot about the SW-cEMI simulation time versus the assembly program lines (L). The green line is the BBTF's simulation time and blue line is rBBTF's. From the plot, we can see the simulation time difference of BBTF and rBBTF method is asymptotically to a constant (the green and blue line become parallel when L is large enough). It show that the $\log(\text{Time}_{\text{BBTF}}) - \log(\text{Time}_{\text{rBBTF}}) = constant$.

Since $\text{speedups} = \frac{\text{Time}_{\text{BBTF}}}{\text{Time}_{\text{rBBTF}}} \approx 1.88$, we can say, by using rBBTF method, rBBTF is about two time faster than BBTF simulation.

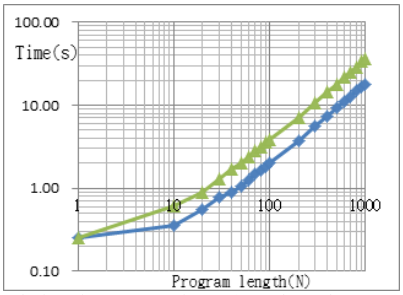

Fig. 11 Simulation time comparisons (speedups) between BBTF and rBBTF

CONCLUSION

This paper proposes a reduced black-box transfer function (rBBTF) method to reduce "internal current activity set" (IntCA set) and "internal PDN impedance set" deduced by black-box transfer function (BBTF) method.

BBTF method can deduce IntCA and IntZ set for software-related conducted EMI (SW-cEMI) modeling at the same time and build a universally accurate SW-cEMI model for target μC within 100 MHz bandwidth.

This paper also presents some measurement result of SW-cEMI of a μC to show that it is no longer a negligible phenomenon for nowadays μC system.

If the μC's machine code set size is N and pipeline stages is p, the size of IntCA/IntZ are both grow linearly with N^p which may be too large for nowadays computer to handle these sets for data processing, indexing, and simulation.

This paper proposes rBBTF method to reduce the IntZ/IntCA set size. The model size reduction ratio, accuracy and speedups are given in this paper. From the experimental results, the proposed method can estimate the SW-cEMI behaviors of a target μC very efficiently without sacrificing much accuracy. Both of the measurement and simulation results are given to justify the claims.

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