

Evaluation Method of Balance Mismatch Using CMRR Measurement for Printed Circuit Board

Mutsumi SHIMAZAKI

Corporate Productivity Engineering Dept.
MITSUBISHI ELECTRIC Corp.

Chiyoda-ku, Tokyo, 100-8310 Japan

Email: Shimazaki.Mutsumi@ds.mitsubishielectric.co.jp

Hideki ASAI

Research Institute of Electronics
Shizuoka University

Hamamatsu-shi, Shizuoka, 432-8561 Japan

Email: hideasai@sys.eng.shizuoka.ac.jp

Abstract—When a primary factor of common-mode noise is corresponding to mismatch of balance on the wiring, the balance degree may be obtained from CMRR (Common Mode Rejection Ratio) of the printed circuit board in the equipment. We calculated CDF(Current Division Factors) as balance degree of micro strip lines. And we showed relational expression of the balance degree and CMRR. By the CMRR measurement, the mismatch of balance between cable and substrate wiring can be evaluated quantitatively.

Keywords—Balance Degree, CDF, CMRR, EMI.

I. INTRODUCTION

When the EMI is emitted from the AC-DC adapter cable of the small electronic device for communication to be used in the home, primary factor of EMI is common-mode noise that is generated by mismatch of balance. We consider the evaluation method of balance-mismatching between the DC power cable and substrate wiring of the printed circuit board. In this report, we analyze character of the balance degree in general substrate wiring, and calculate the balance-mismatching of wiring connected to the cable. Also we show the relationship between the balance-mismatching and CMRR, and measured the CMRR to confirm.

The CMRR measurement is effective in order to evaluate of the balance-mismatching. It can be expected application to prediction of the EMI or common mode generation.

II. THEORY

A. Calculation of balance degree

CDF called balance degree of the transmission line is determined by the cross-sectional structure of the transmission line.[1][2][3] The CDF by cross-sectional structure of the two conductors shown in Fig.1, is calculated by the following formula.[4]

$$h = \frac{C1}{C1 + C2} = \frac{C_{11} + C_{12}}{C_{11} + C_{22} + 2C_{12}} \quad (1)$$

where $C1$ and $C2$ are self-capacitances of the conductors #1 and #2, also C_{11} , C_{12} and C_{22} are the elements of the capacitance matrix defined relationship between two conductors.

As general wiring of the board, we calculated the capacitance matrix of the cross-section model in Fig.2 for seeing the relationship between the balance degree h and Line conductor

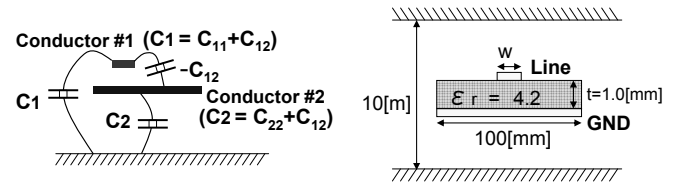


Fig. 1. Capacitances of two conductors

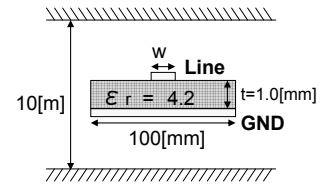


Fig. 2. Cross section model of micro strip line

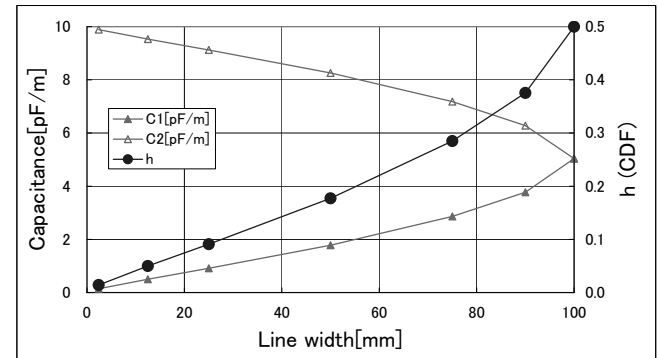


Fig. 3. Balance degree and capacitances of MSL

width of micro-strip line structure. In the computational model, the substrate thickness t is 1.0mm, conductor thickness is 50 μ m, the conductor #1 is Line, and #2 is GND. We used a substrate material such as FR4 ($\epsilon_r=4.2@1\text{GHz}$). Also, in order to avoid the influence of surrounding conductors, the distance to the boundary of the calculation is vertically 5m. This analysis using electromagnetic Field-Solver(HSPICE) of 2D boundary element method has confirmed to be consistent with the calculation result of the model on literature [4].

When the GND conductor width is set to 100mm, and Line width w are from 2.4mm to 100mm, the characteristics of the self-capacitance $C1$, $C2$ and balance degree h are shown in Fig.3. In the case of $w=2.4\text{mm}$, it is micro-strip line (MSL) structure with about 50 Ω characteristic impedance. In the case of $w=100\text{mm}$, it is parallel plate (Plane) structure which the Line and GND width are same. The calculation results of Plane and MSL are respectively

- MSL : $h \approx 0$ (imbalance),

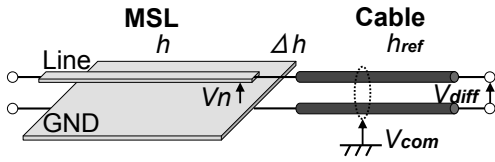


Fig. 4. Connection between MSL and cable

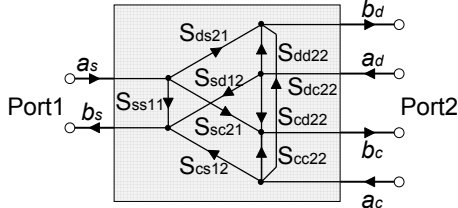


Fig. 5. Mixed-mode S-parameter of splitter

- Plane : $h = 0.5$ (balance),

This degree represents the symmetry of the GND and Line shapes.

B. Relationship between CMRR and balance degree

In the state shown in Fig.4, a cable is connected to the wiring substrate, the relationship between common-mode voltage generation and balance-mismatching can be expressed as follows from the literature [1].

$$\Delta V_c = \Delta h \cdot V_n \quad (2)$$

where input V_n at the MSL is normal mode voltage, ΔV_c is generated common-mode voltage. The Δh for balance-mismatching is shown by the difference between reference h_{ref} and target h .

$$\Delta h = |h_{ref} - h| \quad (3)$$

In this figure, h is CDF for the substrate wiring, and h_{ref} is for the cable. V_{com} and V_{diff} are common-mode and differential-mode voltages of the transmission. Assuming that input voltage V_n is divided to V_{com} and V_{diff} by generated ΔV_c , roughly as below.

$$\begin{aligned} V_{com} &= \Delta V_c = \Delta h \cdot V_n, \\ V_{diff} &= V_n - \Delta V_c = V_n - \Delta h \cdot V_n \end{aligned} \quad (4)$$

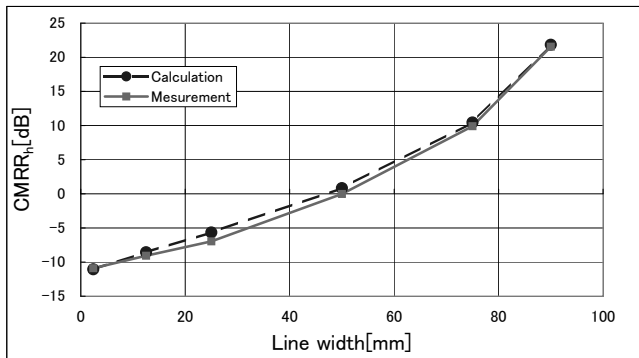


Fig. 6. CMRR of MSL

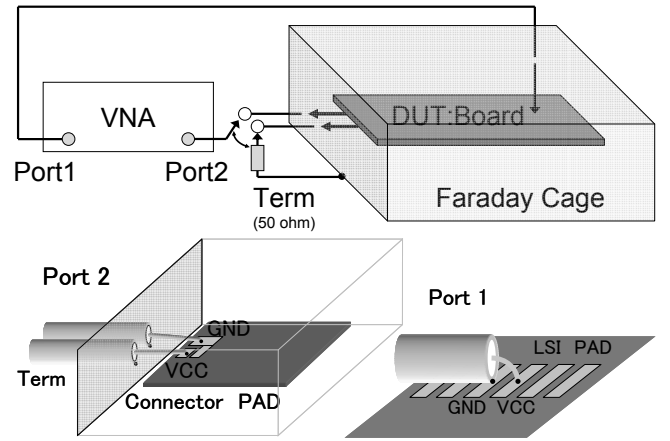


Fig. 7. Proposed measurement system of CMRR

We can consider that substrate wiring is a splitter circuit such as quadrature hybrid for separation to two modes, the properties are defined by the 3port mixed-mode S-parameter of Fig.5. In Fig.5, a is input power, b is output power, s is single-ended signal, d is differential mode signal, c is common mode signal. This S-parameter is expressed below.

$$S_{ds21} = \frac{b_d}{a_s}, \quad S_{cs21} = \frac{b_c}{a_s} \quad (5)$$

Furthermore, CMRR is represented by the power ratio of common-mode and differential-mode, it is indicated by

$$CMRR = \left| \frac{S_{ds21}}{S_{cs21}} \right| = \left| \frac{b_d}{b_c} \right| \quad (6)$$

And the impedances of measurement system are Z_{diff} and Z_{com} . Therefore, these parameters are

$$\begin{aligned} b_d &= \frac{V_{diff}^2}{Z_{diff}} = \frac{(V_n - \Delta h \cdot V_n)^2}{Z_{diff}}, \\ b_c &= \frac{V_{com}^2}{Z_{com}} = \frac{(\Delta h \cdot V_n)^2}{Z_{com}} \end{aligned} \quad (7)$$

Then the relationship between CMRR and balance-mismatching Δh is represented by the following formula.

$$\begin{aligned} CMRR &= \left| \frac{(V_n - \Delta h \cdot V_n)^2 / Z_{diff}}{(\Delta h \cdot V_n)^2 / Z_{com}} \right| \\ CMRR[dB] &= 20 \cdot \log \left| \frac{Z_{com}}{Z_{diff}} \cdot \frac{(1 - \Delta h)^2}{\Delta h^2} \right| \end{aligned} \quad (8)$$

Impedance of the measuring instrument is usually $Z_{diff} = 100\Omega$ and $Z_{com} = 25\Omega$. When it is assumed that h_{ref} is 0.5 as two wires of parallel cable, the CDF of MSL model (Fig.3) can be converted to $CMRR_h[dB]$ (Fig.6 dotted line).

III. EXPERIMENT

On the other hand, in the measurement of single-end S-parameter using VNA (Vector Network Analyzer) and Faraday Cage (Fig.7), CMRR is expressed by the following equation.[5][6]

$$CMRR = \left| \frac{S_{ds21}}{S_{cs21}} \right| = \left| \frac{S_{21} - S_{31}}{S_{21} + S_{31}} \right| \quad (9)$$

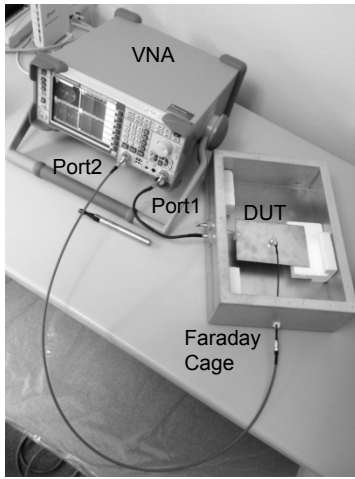


Fig. 8. Measurement set up

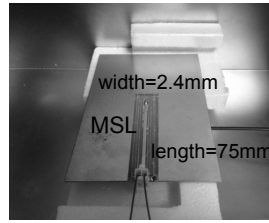


Fig. 9. Test board

We simulated mixed-mode S-parameters of the test board by electromagnetic field solver (HFSS) using a model that enables to simulate the measurement method.[7] For verification, we measured S-parameters of the substrate having a cross-section of MSL(Fig.8). Fig.9 is photo of the test board with the MSL. Also, the results of measurements and simulations are illustrated in Fig.10. In Scs21, Sds21 and CMRR, we were obtained good correlation between the simulation and measurement results.

When the line width w of the MSL used in this model is varied from 2.4mm to 100mm, the simulation results are shown in Fig.11. Although the characteristic of CMRR increases with frequency, the CMRR ratio between every Line width is always constant at each frequency. We regarded this ratio as Δh and converted it into $CMRR_h$ using simple calibration formula(10). It showed perfect agreement to the theoretical value of $CMRR_h$ calculation. (Fig.6 solid line)

$$CMRR_h[dB] = \frac{1}{\rho} \cdot (CMRR_{mes}[dB] + offset_{total}) \quad (10)$$

The causes of difference between theoretical CMRR and original measurements are considered the following three reasons in the measurement system. We can obtain the relational expression(11).

- 1) Relative attenuation ratio
(Calibration ratio: ρ)
- 2) Error of the absolute value
(Correction amount: $offset$)
- 3) Frequency dependence
(Correction function: $f(Frequency)$)

$$CMRR_{mes}[dB] = \rho \cdot CMRR_h[dB] + \sqrt{Freq[MHz]} - offset \quad (11)$$

We suspect that coefficient ρ and $offset$ are depend on the placement conditions of DUT and size of the Faraday Cage to be used in the measurement. In this measurement system case, the parameters are below.

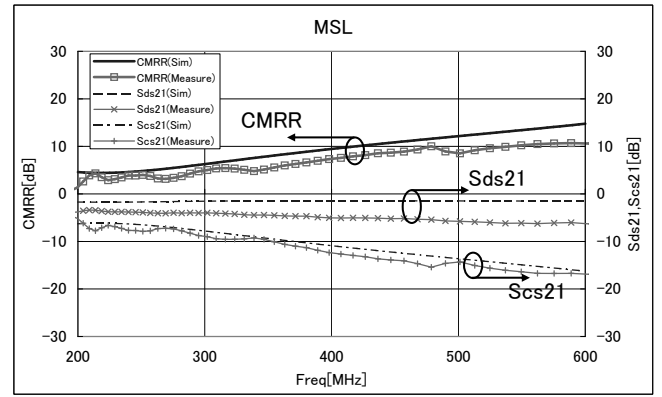


Fig. 10. Comparison between simulation of measurement method and measurement

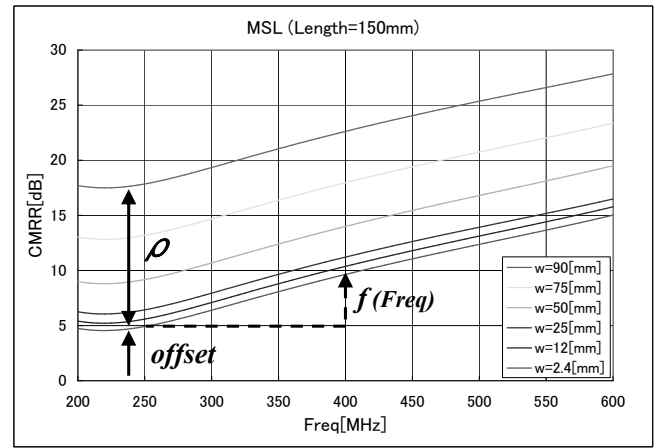


Fig. 11. Simulation results of MSL

$$\rho = 0.4, \quad offset = 6[dB]$$

IV. CONCLUSION

We have shown a formulation of the relationship between CMRR and balance-mismatching Δh . In the CMRR measurement method, it is possible to calculate the Δh from the measurement CMRR by correcting the following relational expression(12).

$$CMRR[dB] = \rho \cdot 20 \cdot \log \left| \frac{Z_{com}}{Z_{diff}} \cdot \frac{(1 - \Delta h)^2}{\Delta h^2} \right| + \sqrt{Freq[MHz]} - offset \quad (12)$$

We are required the theoretical examination about the physical meaning of coefficient ρ , $offset$ and frequency function. Also the relationship of Faraday Cage and these are unknown yet. However, every factor can be identified by the electromagnetic field analysis of the measurement setup. Furthermore, in the design of the circuit board wiring, the measurement of CMRR can be utilized for the comparative evaluation of the amount of balance mismatch.

REFERENCES

- [1] T.Watanabe, O.Wada, T.Miyashita, R.Koga:“Common-Mode-Current Generation Caused by Difference of Unbalance of Transmission Lines on a Printed Circuit Board with Narrow Ground Pattern,”IEICE Trans. Commun., Vol.E83-B, No.3, pp.593-599, March 2000.
- [2] T.Matushima, T.Watanabe, Y.Toyota, R.Koga, O.Wada:“Calculation of Common-Mode Radiation from Single-Channel Differential Signaling System Using Imbalance Difference Model,”IEICE Trans. Commun., Vol.E93-B, No.7, pp.1739-1745, July 2010.
- [3] T.Uno, K.Ichikawa, Y.Mabuchi, A.Nakamura, Y.Okazaki, H.Asai:“An Approach for Practical Use of Common-Mode Noise Reduction Technique for In-Vehicle Electronic Equipment,”IEICE Trans.on Communications, Vol.E93-B, No.7, pp.1788-1796, July 2010.
- [4] T.Watanabe, H.Fujiwara, O.Wada, R.Koga, Y.Kami:“A Prediction Method of Common-Mode Excitation on a Printed Circuit Board Having a Signal Trace near the Ground Edge,”IEICE TRANSACTIONS on Communications, Vol.E87-B, No.8, pp.2327-2334, August 2004.
- [5] W. R. Eisenstadt, B. Stengel, and B. M. Thompson, Microwave Differential Circuit Design Using Mixed-Mode S-Parameters. Boston, MA:Artech House, 2006.
- [6] M.Shimazaki, H.Asai: “ A Study of CMRR Measurement System for Power Distribution Interconnection on Printed Circuit Board,” IEICE Technical Report, Vol.113, No.101, EMCJ2013-19, pp.39-44, June 2013.
- [7] M.Shimazaki, Shinya NISHI, H.Asai: “Evaluation Method of Common-mode Control Using the CMRR in Power Distribution Interconnection on Printed Circuit Board,” Journal of The Japan Institute of Electronics Packaging.,Vol.16, No.4, pp.275-282, Jul. 2013.