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Hetero III-V-N alloy/Si technologies toward monolithic OEIC chips including high-dense light emitting devices

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Structural defect-free Si and InGaPN/GaPN double hetereostructure layers were grown on a Si substrate. Si MOSFETs and LEDs, which are elemental devices for monolithic OEICs, were implemented into a single chip.

1. Introduction

It is essential to grow III-V compound semiconductors on Si substrates for realizing monolithic optoelectronic integrated circuits (OEIC) in which light emitting devices are implemented into Si large-scale integrated circuits (LSI). However, following two problems have to be overcome for realizing the OEIC.

(1) Generation of a large number of structural defects in the growth of III-V compound semiconductors on Si
(2) Mismatch of fabrication processes between Si LSI and III-V compound light emitting devices.

These problems have been overcome [1, 2]. As a result, elemental devices of Si MOSFETs and InGaPN/GaPN DH LEDs for monolithic OEICs were fabricated in Si/GaPN-based epitaxial layers grown on a Si substrate [3].

2. Suppression of structural-defect generation in the growth of Si/(In)GaPN layers on Si substrate

The epitaxial growth of III-V compound semiconductors on Si substrates contains the specific following problems: The differences in (1) the number of valence electrons, (2) lattice parameters and (3) thermal expansion coefficients. These problems cause the generation of structural defects such as dislocations and stacking faults.

Problem (1) causes the generation of anti-phase domains (APDs), stacking faults and threading dislocations at the initial growth stage. This problem was overcome by growing a thin GaP initial layer on a Si (100) substrate misoriented by 4 degree towards a [011] direction at 450 °C by migration-enhanced epitaxy (MEE). Problem (2) generates misfit and threading dislocations in lattice relaxation process. This problem was overcome by lattice-matched growth using GaPN and InGaPN on the GaP initial layer. It should be noted that a lattice parameter decreases with the increase in N compositions x in the III-V-N alloys, while a bandgap (E_g) decreases. Problem (3) could introduce edge dislocations from a grown surface during cooling process after a relatively high temperature growth. This problem was overcome by growing a Si capping layer since tensile strain is negligibly small. Thus, a structural defect-free Si/GaPN layers were realized in principle on a Si substrate, as shown in Fig. 1 [4].

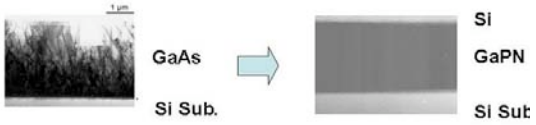

Fig. 1 Structural defect-free Si/GaPN layers grown on a Si substrate [4]

3. Monolithic implementation of MOSFET and LED for OEICs

Elemental devices for the monolithic OEIC are typically a MOSFET and an LED. In principle, the output of a MOSFET circuit is obtained as the light output of the LED. We have tried to fabricate the elemental devices of the MOSFETs in the topmost Si layer and the LEDs in the InGaPN/GaPN DH layer.

The MOSFETs and the LEDs should be fabricated in a conventional processing flow for MOSFETs.

The fabrication processes are shown in Fig. 2 [2]. Thermal process conditions were matched between MOSFETs and LEDs. Wet oxidation was applied to the growth of a gate oxide.

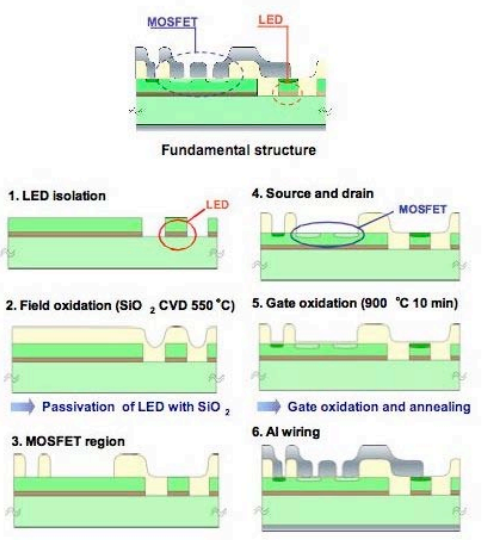

Fig. 2 Fabrication processing flow of elemental devices for a monolithic OEIC [2]

The photograph of a fabricated test chip is shown in Fig. 3, which includes pMOSFETs and LEDs with various sizes [3]. Four LEDs with an active area of 100 μm × 100 μm emitted red light at 10 mA. Drain current I_{ds} vs. drain voltage V_{ds} curves of the pMOSFET with W_g of 30 μm and the spectra of the LED with an active area of 20 μm × 45 μm are inserted in Fig. 3. The optical output of the LED

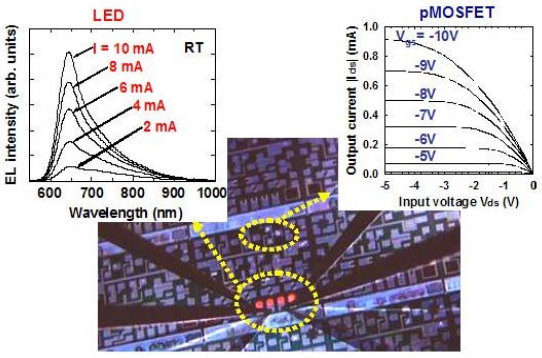

Fig. 3 Photograph of a test chip and device characteristics [3]

was switched by applying a pulsed voltage to the gate of the pMOSFET. OEICs in which LSIs contain a large number of LEDs could be realized when the threshold voltage of MOSFETs is controlled and the small-size LEDs are fabricated. For high performances, point defects should be reduced in (In)GaPN.

4. Summary

Structural defect-free (In) GaPN and layers were grown on a Si substrate. MOSFETs and LEDs, which are elemental devices for OEICs, were monolithically merged in a single chip with a Si layer and an InGaPN/GaPN DH layer grown on a Si substrate. The growth and fabrication process technologies are effective for the realization of monolithic OEICs.

Acknowledgments

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