Study and Analysis of interconnects based on S parameter models

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ABSTRACT: This paper presents study and analysis of interconnects based on scattering parameter (s-parameter) models extracted by full-wave electromagnetic simulation in a CMOS process. This analysis provides well-understanding how back-end layout process affects circuit performance. The analysis of effect of interconnects is investigated in a cascode low-noise circuits for 1.84GHz to 2.5GHz. The metal line between capacitor C_{ex} and inductor L_S or the other line shows the result of effect on the full-wave simulation. This analysis will be helpful to have insight of electromagnetic coupling for more complex interconnects.

1. Introduction

The Complementary Metal-Oxide-Semiconductor (CMOS) process is mainly used for radio frequency integrated circuits (RFICs) due to enormous cost-effectiveness and the opportunity it provides of integrating the RF or millimetre-wave (mm-wave) and digital/analog circuits on a chip. Research for millimetre-wave (30 to 300 GHz) circuits has been concerned with electromagnetic coupling between interconnects [1], [2]. However RF circuits design operating at 1 GHz to 5 GHz is not considered importantly for electromagnetic coupling between interconnects because the dimension of RF circuit on a CMOS process is greatly smaller than its wavelength. Nevertheless, design using a low-resistive bulk silicon ($\rho \sim 10^{-4}\Omega\cdot$cm), which helps preventing latch-up, for digital circuits with the back-end process metal connection or a moderately resistive bulk silicon ($\rho \sim 10\Omega\cdot$cm) for RF or analog circuits are still difficult work part to designers [3]. Many RF circuit designers, therefore, face discrepancy of results of circuit simulation and measurement after fabricating the drawn layout based on circuits. To decrease the discrepancy, some experienced RF circuit designers draw layout from an experienced way, which is achieved by many iterations and time consumed. In addition, electromagnetic coupling effects between metals will become strong as CMOS process is scaled down. In this respect, it shows study of electromagnetic coupling is more import work even for RF frequencies. In this paper, dc s-parameter analysis of Field-Effect transistors (FETs), which needs dc bias, is studied by s parameter extracted by Advanced Design System (ADS), electronic design tool. After completing the dc s-parameter analysis, electromagnetic coupling with different metal line construction is examined from s parameter model extracted by full-wave electro-magnetic (EM) solver. Moreover, to inspect interconnect effects without additional RF device modelling, all RF devices are used with accurate and scalable process design kits (PDKs) provided by TSMC foundry company.

2. Comparison between circuit simulation and DC S-parameter simulation

Theoretically when S-parameters of interconnects obtained at dc or low frequency are used in full-wave simulation, the results should be equivalent to those of conventional circuit analysis where the parasitic coupling effect is not considered. Therefore, the voltage difference of the active component, FET at dc should be checked after ports are properly set in order to analyze properly full-wave simulation with S-parameter. To implement devices as ports, the FET, which is 4 port

device (drain, source, gate, bulk), is modelled in ADS by 3 ports as well as the passive components (i.e. R, L, C) is modelled in ADS by 3ports or 2 ports depending on the topology. As a result, the ADS model counts 37ports. The s-parameter model extracted by ADS is inserted into black box by touchstone format and then RF components are connected to black box as shown in Fig. 2. To confirm a proper dc s-parameter compared to dc bias voltage achieved by the circuit simulator of CADENCE RF spectre, the voltage differences of G1-D1, G1-S1, and D1-S1 of the FETs (i.e. M1, M2) should be checked because the s-parameters do not represent the absolute voltage as the following:

$$\Delta V_n = (a_n + b_n)\sqrt{Z_{0n}}$$
$$and \qquad (1)$$
$$I_n = (a_n - b_n)/\sqrt{Z_{0n}}$$

where n is the port number and Z_{0n} is the characteristic impedance of the port. Table 1 shows the compared results of the voltage difference from dc s-parameter model of Fig. 2 and from circuit schematic of Fig. 1 respectively are identical. This, therefore, shows reasonable start to study full wave EM simulation with s parameter

Table 1: Compared results of circuit simulation and dc S-parameter simulation for FET

unit: [**mV**]

	G1-D1	G1-S1	D1-S1	G2-D2	G2-S2	D2-S2
S-parameter model	34.8176	986.3075	951.4899	-74.343	719.355	793.698
Circuit simulation	34.94	987.541	952.601	-72.459	719.832	792.391

3. Analysis of inter-connection effect using full-wave EM simulation

The cascode LNA circuit designed for general narrow band is used for 2.11-2.17 GHz (WCDMA), 1.84-1.87 GHz (CDMA200 1x), 2.3-2.4 GHz (WiBro) as shown in Fig. 1. The circuit was designed in 0.18μm 1P6M (one-poly six-metal) RF CMOS technology, and the layout of the circuit was drawn as shown in Fig. 3(a). The S_{21}, S_{11} of circuit simulation was different from the S_{21}, S_{11} caused by effect of electromagnetic, which is achieved by EM simulation, in Fig.5. The S_{11} with EM simulation was shifted to a higher frequency and S_{21} to a lower frequency than those of conventional circuit simulation as show in Fig. 5. To analyze this result, the passive and active components are removed from the layout. Then the deleted components are replaced with π shape ports in Fig 4. “A”, “B” and “C” in Fig. 4 are expressed as port. “A” contains series of passive models and “B”, “C” contains substrate shunt of passive models in PDK. To investigate the effect of electromagnetic coupling of interconnects, the different interconnects of the layout (e.g. path between L_s-C_{ex} and between L_g-C_{ex}) were observed in Fig. 3(b), (e) respectively. In L_s-C_{ex} of the layout, there are two parallel lines side by side between L_s and C_{ex}. The two metals combine together by position of edge of C_{ex} from L_s. This makes effect to reduce the electromagnetic coupling between the metals as well as self-parasitic (RLC) in Fig.5. This effect shows the parasitic capacitor C_{eff} appeared by EM effect in Fig.3 (a) decreases and thus reduced value of C_{ex} by C_{eff} get increased. As a result, it shows S_{11} with EM simulation of Fig. 3 (b) is shifted to lower frequency than S_{11} of Fig. 3 (a) in Fig. 5. In L_g-C_{ex} of the layout, there is the 6-metal line between Lg and gate of FET (M1). By means of increasing the line in this time, the electromagnetic coupling between L_g-C_{ex} could increase. This changed line confirms facts of raised electromagnetic coupling from result of that adding C_{eff} between L_g-C_{ex} in the circuit of Fig. 3 (f) makes S_{11} shifted to lower frequency. The result of S_{11} with EM effect in Fig. 3 (f) shows it is moved to the lower frequency than S_{11} in Fig. 3 (d). In addition, the LNA using simultaneous noise and input matching (SNIM) [4] by changed S_{11} influences noise figure (NF) seriously. Therefore, this paper shows the electromagnetic coupling effect even for 1GHz to 5GHz can influence critical circuit performance. In this respect, it shows this analysis and study will be helpful to optimize layout and thus

predictable result of circuit simulation can be achieved without time consuming iteration work for much more complex metals.

4. Conclusion

In this paper, RF interconnect arrangement is studied and analyzed to predict layout effect based on s-parameter. The results of dc S-parameter simulation and dc circuit simulation shows proper start to analyze full-wave EM simulation. The circuit simulation with full-wave EM simulation shows a change of about 7.5% and 18%, for S_{11} and S_{21}, respectively. These variations also influence overall circuit performance. Therefore optimizing layout by means of full-wave simulation based on s-parameter before fabrication can reduce time-consuming repetition of trial and error.

Acknowledgments

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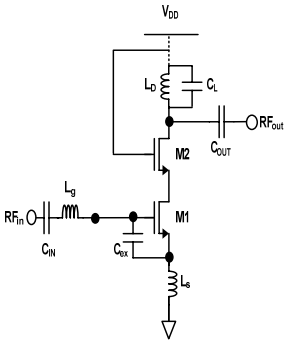


Figure 1: A cascode LNA schematic

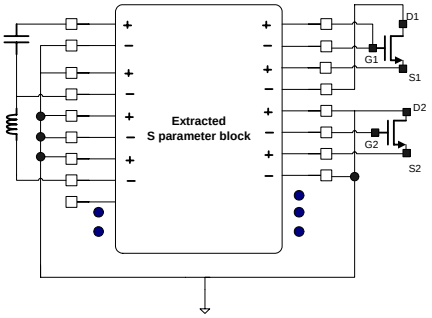
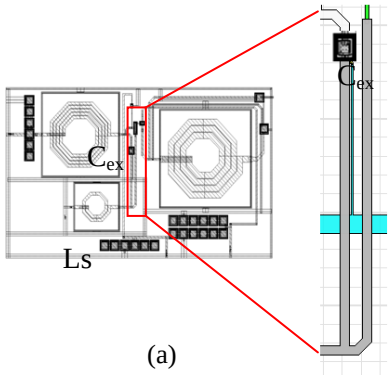
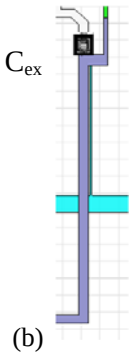


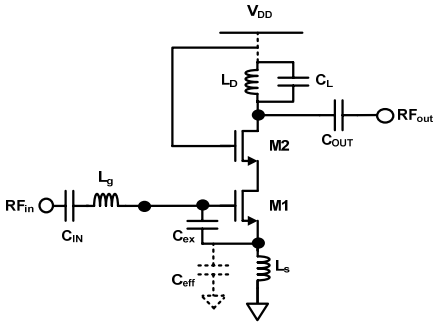
Figure 2: Circuit analysis with interconnect effect included in s-parameter



(a)



(b)



(C)

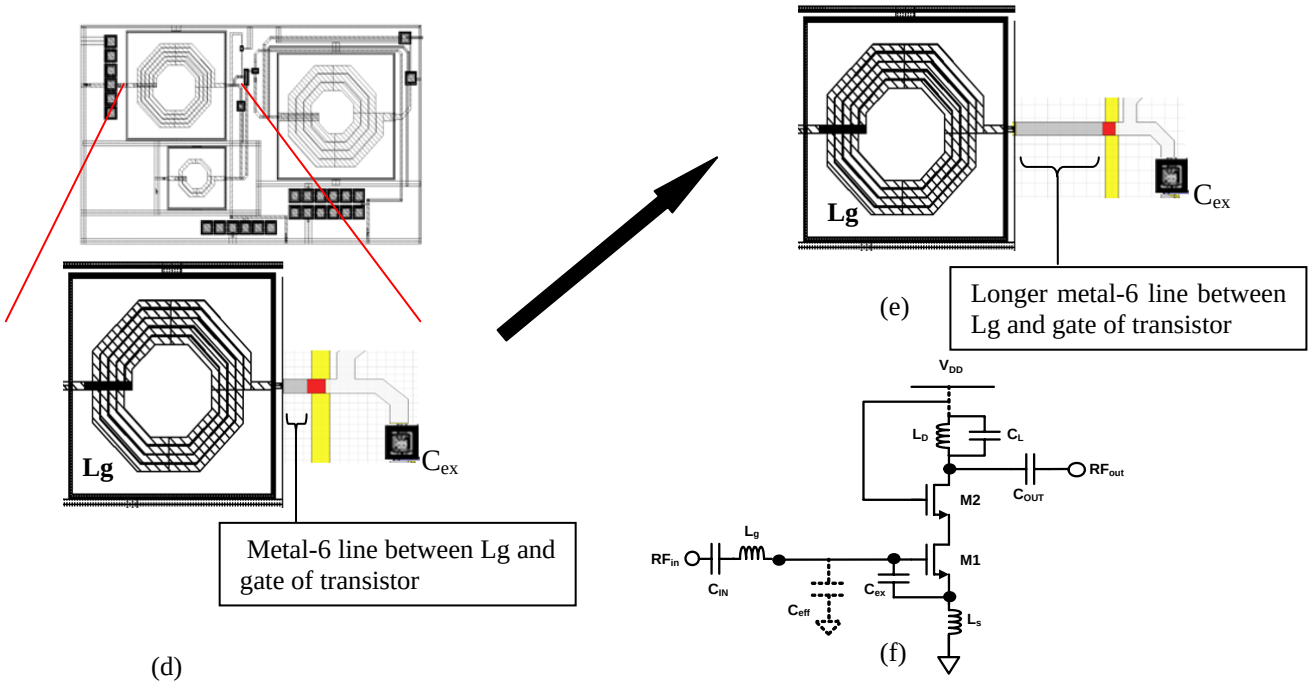


Figure 3: The layout of the designed LNA (a) Before layout modified in the interconnect between C_{ex} and L_s (b) After layout modified in the interconnect between C_{ex} and L_s (c) the effect of layout in the circuit (d) Before layout modified in the interconnect between C_{out} and drain (e) After layout modified in the interconnect between C_{out} and drain (f) the effect of layout in the circuit

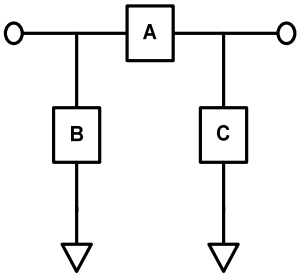


Figure 4**:** π shape ports

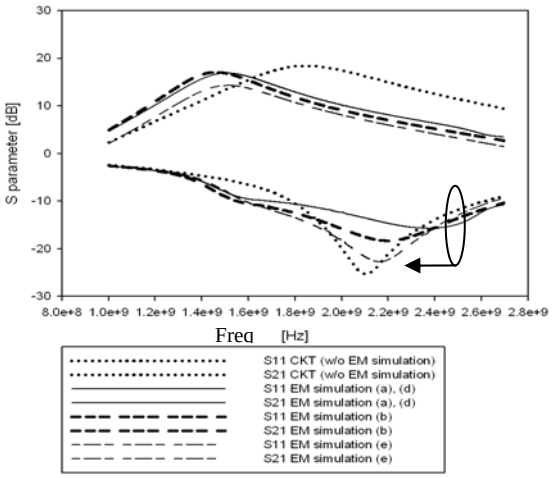


Figure 5: S_{11} and S_{21} of the circuit simulation and EM simulation

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