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A Charge-Based SiC Power MOSFET Model Considering On-State Resistance

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Abstract—Transistor models have been playing a key role in designing efficient power converters. As the operating frequency of the converters becomes higher, transistor models need to represent physical device behavior accurately and compactly. In this paper, we propose a charge-based transistor model that considers gradual transition between linear and saturation regions, and parasitic resistances of vertical diffused SiC power MOSFET. Transient simulation using the proposed model, as well as I-V and C-V characteristics, matched well with the experimental results using a commercial device.

1. Introduction

Silicon Carbide (SiC) is considered as one of the most promising materials for realizing power converters that operate with high power density and at a high frequency. Accurate circuit simulation is crucial to optimally design power converters. The simulation accuracy greatly depends on the accuracy of the SiC power device model.

Fitting-based equations have been widely used as the SiC power MOSFET model [1]. These models are recognized to efficiently simulate the electrical behavior of the SiC power MOSFET. However, in such models, prediction of the physical phenomena, such as process variation and reliability of SiC, is difficult because the mathematical model does not contain physically meaningful parameters that actually varies in real devices. Also, the characteristics outside the fitting region may not be sufficiently accurate.

Recently, inversion charge-based transistor models have been successfully applied for designing silicon-based integrated circuits. The charge-based models can accurately reproduce behavior of silicon devices computationally efficiently [2, 3]. However, charge-based model has not yet been applied to the models of SiC vertically double diffused MOSFETs (VDMOSFETs). Model equations have to be modified to represent I-V characteristics. In particular, parasitic resistances associated with the vertical current flow in the vertical double diffused structure have to be accurately modeled.

In this paper, we propose an accurate SiC power MOSFET model based on the channel charge. The proposed model takes into account the bias dependence of the parasitic resistances of the VDMOSFET. The capacitance characteristics are represented by the analytic expressions proposed in [4]. The I-V, C-V, and transient characteristics of the proposed model have been validated through experiments using a commercial SiC device.

2. Charge-Based Model

The charge-based model is a compact device model that is widely used for simulating silicon-based MOSFETs. On the basis of single equation, the charge-based model can accurately and consistently predict the circuit performance [2, 3]. No concatenation of separate equations is required to represent full operational range of the device. This is one of the advantages over the conventional models, such as [5]. Another advantage of the charge-based model is its efficiency. The drain current is accurately obtained through an analytic expression that represents inversion charge density at the source and drain electrodes.

We adopt EKV model [2] as the basis of our proposed model. The drain current I_{DS} is represented as [6]:

$$I_{DS} = \beta \int_{V_S}^{V_D} \frac{-Q_i}{C_{OX}} dV. \quad (1)$$

Here, V_D and V_S are drain and source voltages, respectively. $\beta = \mu C_{OX} \frac{W}{L}$ is the transmission coefficient, being L the channel length, W the channel width, μ the carrier mobility, and C_{OX} the oxide capacitance per unit area. Although Eq. (1) is an accurate expression of the physical current flow, it involves numerical integration of the inversion charge Q_i. Its computational cost is in general too high for use as the compact device model. In the EKV model, the inversion charges at the drain and source ends of the channels are approximated to facilitate analytic calculation. With this approximation, the drain current is obtained with a small calculation time.

The EKV model considers the inversion charge Q_i in both strong and weak inversion regions. When the body effect is sufficiently small, by solving the Poisson's equation at the surface of the channel, the inversion charge is written as

$$\begin{aligned} Q_i(strong\ inv.) &\simeq -nC_{OX}(V_P - V_{ch}), \\ Q_i(weak\ inv.) &\simeq -K_w C_{OX} U_T \exp\left(\frac{V_P - V_{ch}}{U_T}\right). \end{aligned} \quad (2)$$

Here, V_P is the pinch-off voltage, V_{ch} is the electric potential in the channel, and U_T is the thermal voltage. In addition, $n \equiv 1 + \gamma/(2\sqrt{\Psi_0 + V_{ch}})$ and $K_w \equiv (n -$

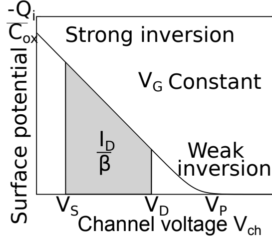

Figure 1: Drain current according to Eq. (4).

$1)\exp\{(\Psi_0 - 2\Phi_F)/(U_T)\}$. γ is the substrate bias factor, Ψ_0 is the channel surface potential at $V_{ch} = 0$, Φ_F is the Fermi potential, and V_{T0} is the threshold voltage at the zero bias. The pinch-off voltage V_P is defined as follows:

$$V_P = V_G - V_{T0} - \gamma\left[\sqrt{V_G - V_{T0} + \left(\frac{\gamma}{2} + \sqrt{\Psi_0}\right)^2} - \left(\frac{\gamma}{2} + \sqrt{\Psi_0}\right)\right]. \tag{3}$$

Figure 1 illustrates the surface potential as a function of V_{ch} at a constant gate voltage V_G. V_{ch} varies from zero to V_P, and the surface potential also changes according to V_{ch}.

The current that flows from the source to the drain (forward current I_F) is obtained by integrating Q_i/C_{OX} from V_S to infinity. Similarly, by integrating from V_D to infinity, the current from the drain to the source (reverse current I_R) is obtained. Because the drain current I_{DS} is the difference between I_F and I_R, I_{DS} can be expressed as follows:

$$I_{DS} = I_F - I_R = \underbrace{\beta\int_{V_S}^{\infty}\frac{-Q_i}{C_{OX}}dV}_{\text{Forward current } I_F} - \underbrace{\beta\int_{V_D}^{\infty}\frac{-Q_i}{C_{OX}}dV}_{\text{Reverse current } I_R}. \tag{4}$$

In order to calculate I_{DS} by Eq. (4), I_F, I_R, and the transition between I_F and I_R need to be modeled. I_F and I_R can be derived from Eq. (2). In the EKV model, the smoothing function is introduced to fit the transition.

3. Charge-Based SIC Power MOSFET Model

3.1. Overview of the Proposed Device Model

In this section, the proposed charge-based SiC power MOSFET model is explained. Figure 2 shows the structure of the proposed model. The drain current I_{DS} is expressed based on the charge-base model described in Sec. 2.

The proposed model assumes the VDMOSFET structure shown in Fig. 3. The VDMOSFET has the parasitic resistances on its current path, total of which is on-resistance R_{on}. The value of each resistance is voltage dependent. Hence, all voltage dependencies of the on-resistances has to be correctly modeled in order to accurately simulate the current characteristic of the SiC power MOSFET.

The parasitic capacitances, C_{GS}, C_{DS}, and C_{GD}, are also modeled considering the dependencies to the drain-source voltage V_{DS} and the gate-source voltage V_{GS}. In the proposed model, the capacitance model proposed in [4] is used.

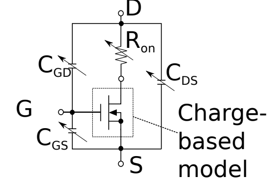

Figure 2: Structure of the proposed model.

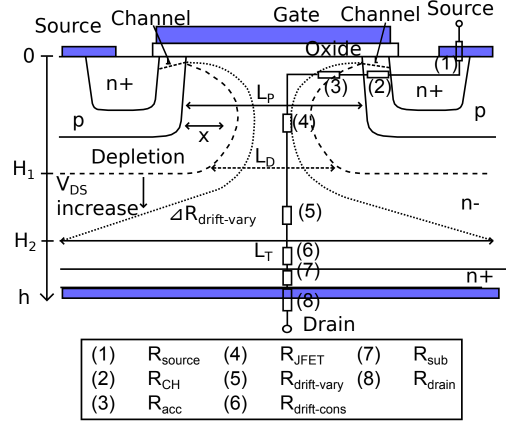

Figure 3: Cross section of the VDMOSFET with parasitic resistances.

3.2. Drain Current Model

In order to apply the charge-based model to SiC VDMOSFETs, the following changes have been made.

- Mobility degradation due to interface traps at the SiC/SiO_2 [7] has been considered.
- Bias-dependent on-resistances of VDMOSFET [8, 9] have been considered.

According to the measurement results of the drain current of SiC power MOSFETs, the transition between linear and saturation regions occurs more gradually than silicon transistors. The smooth transition is considered to be caused by high density of interface states in the inversion channel [7]. When body effect coefficient is sufficiently small, Eq. (3) can be rewritten as $V_P = V_{GS} - V_{T0}$. However, this equation is insufficient to express the gradual transition. Through the observations on the measured I-V characteristics, we found that the gradual transition can be modeled by modifying the pinch off voltage as:

$$V_P = N_{GS}(V_{GS} - V_{T0})^{\alpha} + N_{DS}[(V_{GS} - V_{T0})^2 V_{DS}]^{\zeta}, \tag{5}$$

where N_{GS}, N_{DS}, α, and ζ are fitting parameters.

Figure 3 shows the cross section of the VDMOSFET. The on-resistance R_{ON} for this vertical structure is defined by considering the following resistances: source terminal resistance R_{source}, drain terminal resistance R_{drain}, substrate resistance R_{sub}, accumulation resistance R_{acc}, channel resistance R_{CH}, JFET resistance R_{JFET}, constant drift region resistance $R_{drift-cons}$, and variable drift region resistance

$R_{\text{drift-var}}$. Here, R_{source}, R_{drain}, $R_{\text{drift-cons}}$, and R_{sub} are constant resistances determined by the geometry of the VD-MOSFET.

R_{acc} is the variable resistance. According to [8], due to the charge density of accumulation layer, R_{acc} becomes V_{GS} dependent

$$R_{\text{acc}} = \frac{1}{\frac{W}{L}\mu C_{\text{ox}}(V_{\text{GS}} - V_{\text{T0}})}. \tag{6}$$

R_{JFET} is also the variable resistance formed at the JFET region. R_{JFET} limits the drain current path by the width of the depletion layer that depends on V_{DS}. R_{JFET} can be written as

$$R_{\text{JFET}} = \frac{\rho l}{L_{\text{D}} W}. \tag{7}$$

L_{D} is the distance between depletion layers, and it is defined as $L_{\text{D}} = L_{\text{P}} - 2x$. Here, L_{P} is the distance between adjacent p regions. W is the channel width, l is the vertical depth of the JFET region, and ρ is the receptivity of the JFET region. $L_{\text{D}}W$ expresses the cross-sectional area of the JFET region. The width of the depletion layer x is given as

$$x = \sqrt{\frac{2\varepsilon_{\text{sic}}}{q}\frac{N_{\text{A}} + N_{\text{D}}}{N_{\text{A}}N_{\text{D}}}(V_{\text{bi}} + V_{\text{DS}})}, \tag{8}$$

where V_{bi} is the built-in voltage, ε_{SiC} is the permittivity of SiC, q is the elementary charge, and N_{D} and N_{A} are the densities of donors and acceptors, respectively. By applying V_{DS}, L_{D} changes. Combining the above equations, R_{JFET} becomes:

$$R_{\text{JFET}} = \frac{\rho h}{L_{\text{D}} W} = \frac{\rho h}{\left(L_{\text{P}} - \sqrt{\frac{2\varepsilon_{\text{sic}}}{q}\frac{N_{\text{A}}+N_{\text{D}}}{N_{\text{A}}N_{\text{D}}}(V_{\text{bi}} + V_{\text{DS}})}\right) W}. \tag{9}$$

In the model of $R_{\text{drift-vary}}$, H_1 and H_2 are defined as the depths from the substrate-surface of the device.

As shown in Fig. 3, by supposing s as the cross-sectional area of the $R_{\text{drift-vary}}$ between H_1 and H_2, $R_{\text{drift-vary}}$ can be expressed as follows:

$$R_{\text{drift-vary}} = \int_{H_1}^{H_2} \frac{\rho}{s} \mathrm{d}h,\ s = W\left(L_{\text{D}} + \frac{L_{\text{T}} - 2L_{\text{D}}}{H_2} l\right). \tag{10}$$

where L_{T} is the distance between adjacent source terminals. Therefore, Eq. (10) can be rewritten as follows:

$$\begin{aligned} R_{\text{drift-vary}} &= \int_{H_1}^{H_2} \frac{\rho}{W\left(L_{\text{D}} + \frac{L_{\text{T}}-2L_{\text{D}}}{H_2} l\right)} \mathrm{d}h \\ &= C_1 V_{\text{DS}} + \log(V_{\text{DS}}) + C_2 V_{\text{DS}} + C_3. \end{aligned} \tag{11}$$

Here, C_1, C_2, and C_3 are the coefficients represented by using device dimensions and physical parameters.

The on-resistance R_{ON} of the VDMOSFET is considered as the series connection of all the above parasitic resistances. Thus, by arranging the sum of the parasitic resistances as N_1–N_5, R_{on} is expressed as follows:

$$R_{\text{on}} = \frac{N_1}{(V_{\text{GS}} - V_{\text{T0}})} + N_2 V_{\text{DS}}^{\zeta} + \frac{N_3}{N_4 - \sqrt{V_{\text{DS}} + V_{\text{bi}}}} + N_5. \tag{12}$$

Table 1: Model parameters of current characteristic

Parameter	Explanation	Value
Ψ_0 [V]	Surface potential when $V_{\text{ch}} = 0$	6.22
V_{T0} [V]	Threshold voltage at zero bias	5.31
N_{GS}	Coefficient of V_{P} on V_{GS}	1.81×10^{-1}
α	Multiplier of V_{P} on V_{GS}	1.60
N_{DS}	Coefficient of V_{P} on V_{DS}	7.52×10^{-4}
ζ	Multiplier of V_{P} on V_{GS}	1.13
μC_{ox}	Transconductance	3.61×10^{-3}
N_1	$\frac{W}{L\mu C_{\text{OX}}}$	8.79×10^{-3}
N_2	Coefficient of $R_{\text{drift-vary}}$	1.50×10^{-2}
N_3	$\rho l\sqrt{\frac{qN_{\text{A}}N_{\text{D}}}{2\varepsilon_{\text{sic}}(N_{\text{A}}+N_{\text{D}})W}}$	1.09
N_4	$C\sqrt{\frac{qN_{\text{A}}N_{\text{D}}}{2\varepsilon_{\text{sic}}(N_{\text{A}}+N_{\text{D}})}}$	41.27
$N_5[\Omega]$	Fixed resistance	2.09×10^{-1}

Table 2: Model parameters of capacitance characteristic

Parameter	Explanation	Value
V_{bi} [V]	Built-in voltage	2.01
V_{td} [V]	Threshold drain voltage	5.52×10^{-1}
$C_{\text{GS}}(0)$ [F]	C_{GS} at zero bias	5.38×10^{-10}
$C_{\text{DS}}(0)$ [F]	C_{DS} at zero bias	3.07×10^{-10}
$C_{\text{GD}}(0)$ [F]	C_{GD} at zero bias	2.23×10^{-10}
C_{oxd} [F/Vs]	Gate-drain oxide capacitance	4.11×10^{-3}

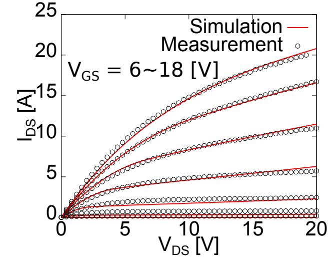

Figure 4: I_{DS}-V_{DS} characteristics.

4. Experimental Results

The proposed device model is validated using a commercial SiC power MOSFET (1200V, 10A, [10]). I-V and C-V characteristics of the SiC power MOSFET are measured by a commercial curve tracer [11]. The proposed device model is implemented by Verilog-A. I-V, C-V, and transient characteristics are calculated by a commercial circuit simulator [12]. Model parameters are determined by a simulated annealing method [13]. The Model parameters used in the proposed model for I-V and C-V characteristics are summarized in Table 1 and 2, respectively.

4.1. I-V and C-V Characteristics

The measured and simulated current and capacitance characteristics are compared in Figs. 4 and 5. In Fig. 4, V_{GS} is varied from 6 V to 18 V with a 2 V step. In Fig. 5, capacitance values are measured from $V_{\text{DS}} = 0$ V to $V_{\text{DS}} =$

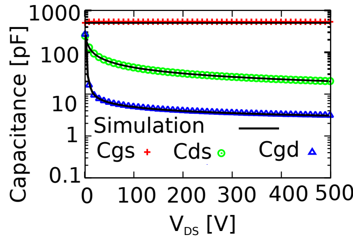

Figure 5: C-V_{DS} characteristics.

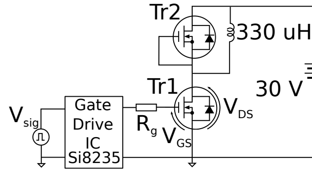

Figure 6: Circuit schematic of double pulse tester.

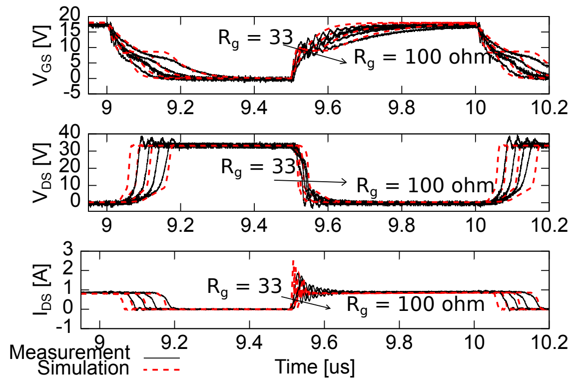

Figure 7: Measured (solid) and simulated (dashed) waveforms.

500 V. The fitting results of the proposed model agree very well with the measurement. Through the adjustment of V_{P} and parasitic resistances in the preceding chapter, the mean square error of current characteristic is reduced to 0.24 A.

4.2. Transient Characteristic

The transient characteristic is evaluated using a double pulse tester circuit shown in Fig. 6. The switching frequency is 1 MHz and the pulse duty factor is 50%. The gate series resistance R_{g} is varied as 33, 47, 68, and 100 Ω. Figure 7 shows both simulated (solid black) and measured (dashed red) waveforms at turn-on and turn-off periods. The proposed model can accurately simulate the switching waveforms of the SiC power MOSFET for all R_{g} values.

But simulation wave pattern of V_{DS}, I_{DS} is earlier than measurement. It is thought that this does not consider the parasitic ingredient in the actual survey circuit by the circuit simulation of this experiment.

5. Conclusion

In this paper, we proposed a charge-based model for SiC power devices considering the structure of the VDMOSFET. The proposed model also takes into account the gradual transition between linear and saturation regions due to interface traps. Experimental results using a commercial SiC power MOSFET show that the proposed simulation model accurately reproduces I-V, C-V, and transient characteristics.

Acknowledgments

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