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Design Example of SiC Isolated Soft-Switching Driver

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Abstract—This paper proposes an isolated resonant gate driver for SiC MOSFETs. By applying the class-E zero-voltage switching and zero-derivative switching (ZVS/ZDS) conditions, the proposed driver achieves high power-conversion efficiency at high frequencies. An analysis and a design example of the proposed driver are presented along with simulation and experimental results.

1. Introduction

Recently, Silicon Carbide (SiC) devices attract attentions as a next generation semiconductor devices [1]-[6]. SiC power devices can maintain high performance with high power. This is because SiC power devices have characteristics of high breakdown voltage and low thermal resistance. In most cases, SiC applications are considered at up to hundred kHz order. It is a challenging problem to use SiC devices at MHz-order frequencies.

The design of driver circuit is one of the important and difficult problems for operating SiC devices at high frequencies. Recently, gate drivers for high frequency operations of SiC MOSFETs [1]-[3] have been presented. The power loss at the driver is, however, cannot be ignored because of the hard switching. Additionally, the rectangular drive voltage strains due to parasitic capacitances and resistance on SiC devices.

It is one of the solutions to include the parasitic capacitance in the output resonant filter of the driver and the MOSFET is driven by the sinusoidal signal [7]-[10]. This is called as resonant driver. It is also an advantage of the resonant driver that the soft switching techniques can be adopted. Namely, the power-conversion efficiency is enhanced. It is, however, required that the output filter includes isolation topology for safety drive of the SiC.

This paper proposes an isolated resonant gate driver for SiC MOSFETs. The proposed driver includes a transformer for the isolations. In addition, the class-E zero-voltage switching and zero-derivative switching (ZVS/ZDS) conditions at turn-on instants are applied to the driver switch. Because of the class-E ZVS/ZDS conditions, the proposed driver achieves high power-conversion efficiency at high frequencies. An analysis of the proposed driver is carried out and a step-by-step design procedure based on the obtained analytical expressions is presented. As a design example, resonant SiC driver for 7 MHz operation is designed. The validity of the analytical expressions and design procedure were confirmed from the quantitative agreements with experimental and PSpice-simulation results.

2. Proposed Gate Driver

Figure 1 shows a proposed SiC gate driver. The basic topology is the class-E amplifier, which consist of input voltage V_D, dc-feed inductance L_C, MOSFET S as a switching device, shunt capacitance C_S, and output filter. In the proposed driver, the isolation transformer is applied as shown in Fig. 1(a). The transformer is modeled the primary inductance L_1 and secondary inductance L_2 with mutual inductance M and equivalent series resistances (ESRs) of the coupling inductances r_{L1} and r_{L2}. The primary side of the output filter is composed of C_1, C_p and L_1, where C_p is a component for adjusting the amplitude of the drive voltage. The secondary side of the output filter has L_2 and C_2, which is connected to gate of SiC MOSFET in series. The gate of the SiC is modeled as the gate capacitance and gate resistance, which are connected in series as shown in Fig. 1(b). Therefore, C_2 has a role to make an impedance matching at the secondary part. It is important to consider ESRs of the coupling inductances for considering the power-conversion efficiency optimization. Note that the gate voltage is the sum of the voltages across the C_g and R_g.

Figure 2 shows example waveforms of the proposed gate driver, where $\theta = \omega t = 2\pi f t$ is the angular time and f is the operating frequency. When the switch is in ON state, the switch voltage is approximately zero. Conversely, current flows through the shunt capacitance when the switch is OFF state, which produces the pulse-type shape of switch voltage v_S. The most important operation of the proposed driver is to achieve the class-E ZVS/ZDS conditions at the turn-on instant of switch voltage as shown in Fig. 2. Namely, the switch voltage satisfies

$$v_S(2\pi) = 0 \ \text{ and } \ \left.\frac{dv_S(\theta)}{d\theta}\right|_{\theta=2\pi} = 0, \qquad (1)$$

simultaneously. Because of the class-E ZVS/ZDS conditions, the proposed driver achieves high power-conversion efficiency at high frequencies.

It is expected that a sinusoidal current flows through the output filter as shown in Fig. 2. This is because it is easy to control the duty ratio. For obtaining the sinusoidal output current, it is important to keep high loaded quality factor at the output filter. The gate capacitance C_g and gate resistance R_g, however, are not small at SiC MOSFET, which is hard condition for achieving high Q. This is a reason why the capacitance C_2 is added in the secondary part. By adding C_2, it is possible to reduce the resonant capacitance in the secondary part. Namely, high Q output

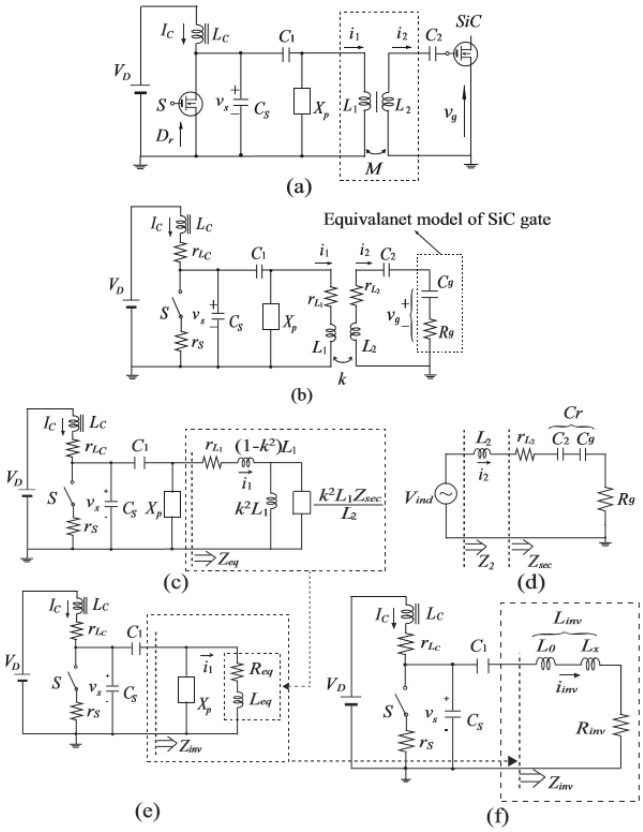

Figure 1: Proposed resonant gate driver using class-E inverter for SiC MOSFET. (a) Circuit topology. (b) Equivalent circuit. (c) Equivalent circuit of the primary part. (d) Equivalent circuit of the secondary part. (e) Equivalent circuits boiled down to the primary part. (f) Equivalent circuits boiled down to the secondary part.

filter for obtaining a sinusoidal output current can be realized.

From above discussions, it is seen that the design of the secondary part is focused on the impedance matching. For gate-driver applications, it is important to adjust the output voltage of the gate signal for satisfying the maximum/minimum gate voltage conditions. Therefore, the impedance transform component C_p is also mandatory component for designing the gate driver.

It is necessary to obtain a set of component values for achieving the class-E ZVS/ZDS conditions and specified amplitude of the gate voltage, which is a problem of the proposed driver designs. The circuit analysis is effective way to solve this problem.

3. Analysis of Proposed Driver

In this section, the analytical expressions of the proposed driver are given. The analytical expressions are necessary to design the proposed circuit with achieving the class-E ZVS/ZDS conditions.

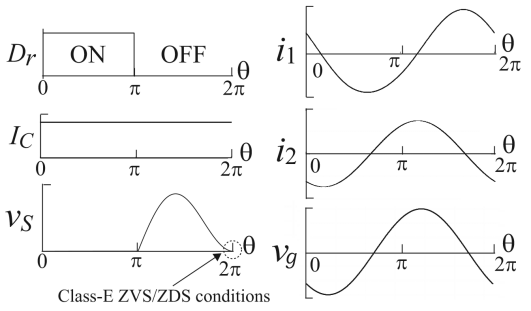

Figure 2: waveforms of proposed resonant gate driver.

3.1. Secondary Part

The current thorough the secondary part is expressed as

$$i_2 = I_2 \sin(\theta + \phi_r), \tag{2}$$

where I_2 and ϕ_r are the amplitude of i_2 and the phase shift between the driving signal of the switching device D_r and the input current of the secondary part i_2. The amplitude of the secondary current is obtained from

$$I_2 = \frac{V_g}{|Z_g|} = \frac{V_g}{\sqrt{R_g^2 + \left(\frac{1}{j\omega C_g}\right)^2}}, \tag{3}$$

where V_g is amplitude of gate voltage. The equivalent capacitance of the secondary part is

$$C_r = \frac{C_g C_2}{C_2 + C_g}. \tag{4}$$

The power-conversion efficiency is maximized when the resonant circuit at the secondary part is resonated with operating frequency f [11], namely

$$C_r = \frac{1}{\omega^2 L_2}. \tag{5}$$

Therefore, the secondary resonant capacitance is fixed as

$$C_2 = \frac{C_g}{\omega^2 L_2 C_g - 1}. \tag{6}$$

The loaded quality factor of the resonant circuit is defined as

$$Q_2 = \frac{\omega L_2}{R_g}, \tag{7}$$

which is used for obtaining the sinusoidal output.

3.2. Coupling Part

From C_r and R_g, the impedance Z_2, which is defined in Fig. 1(d), is expressed as

$$Z_2 = r_{L_2} + R_g. \tag{8}$$

From (8), the amplitude of induced voltage from the primary part can be obtained as

$$V_{ind} = |Z_2| I_2 = (r_{L_2} + R_g) I_2. \tag{9}$$

In this analysis, the equivalent transformer model in Fig. 1(c) is adopted, where Z_{sec} is defined as the impedance as shown in Fig. 1(d), namely,

$$Z_{sec} = r_{L_2} + R_g + \frac{1}{j\omega C_r}. \tag{10}$$

Dotted-line part in Fig. 1(c) is transformed into equivalent resistance and inductance connected in series as shown in Fig. 1(e). From (10), the impedance of Z_{eq} in Fig. 1(c) is

$$\begin{aligned} Z_{eq} &= \frac{\omega^2 k^2 L_1 L_2 Z_2}{Z_2^2 + \left(\omega L_2 - \frac{1}{\omega C_2}\right)^2} + r_{L_1} \\ &+ j\omega \left[\frac{k^2 L_1 \left(Z_2^2 - \frac{L_2}{C_2} + \frac{1}{\omega^2 C_2^2} \right)}{Z_2^2 + \left(\omega L_2 - \frac{1}{\omega C_2}\right)^2} + L_1(1-k^2) \right] \\ &= \frac{k^2 \omega^2 L_1 L_2}{R_g + r_{L_2}} + r_{L_1} + j\omega L_1 \end{aligned} \tag{11}$$

Therefore, the equivalent resistance R_{eq} and the equivalent inductance L_{eq} are

$$R_{eq} = \frac{k^2 \omega^2 L_1 L_2}{R_g + r_{L_2}} + r_{L_1} \tag{12}$$

and

$$L_{eq} = L_1. \tag{13}$$

3.3. Primary part

From the above analysis, the equivalent circuit of the proposed circuit is illustrated as shown in Fig. 1(e). The current through the primary coil I_1, which is the amplitude of i_1, can be calculated from

$$I_1 = \frac{V_{ind}}{\omega k \sqrt{L_1 L_2}} = \frac{(r_{L_2} + R_g) I_2}{\omega k \sqrt{L_1 L_2}}. \tag{14}$$

For achieving the specified drive voltage and the class-E ZVS/ZDS conditions at turn-on instants, Z_{eq} is transformed into $Z_{inv} = R_{inv} + jL_{inv}$ by the impedance transformation capacitance C_p as shown in Fig. 1(f). R_{inv} and L_{inv} are obtained as [11]

$$R_{inv} = \frac{R_{eq}}{\omega^2 C_p^2 \left[R_{eq}^2 + \left(\omega L_{eq} - \frac{1}{\omega C_r} \right)^2 \right]}, \tag{15}$$

and

$$L_{inv} = \frac{L_{eq}(1 - \omega^2 L_{eq} C_p) - C_p R_{eq}^2}{\omega^2 C_p^2 \left[R_{eq}^2 + \left(\omega L_{eq} - \frac{1}{\omega C_r} \right)^2 \right]}, \tag{16}$$

respectively, where D is the on-duty ratio of switch S, ϕ_{inv} is the phase shifts between the driving signal D_r and the inverter current i_{inv}. ϕ_{inv} is [12],

$$\phi_{inv} = \pi + \tan^{-1} \frac{\cos(2\pi D) - 1}{2\pi(1-D) + \sin(2\pi D)}. \tag{17}$$

L_{inv} is divided into L_0 and L_x, where L_0 and C_1 realize resonant circuit for operating frequency f. Therefore, L_x, which is used for current phase shift for achieving the class-E ZVS/ZDS conditions, can be obtained as

$$\begin{aligned} \frac{\omega L_x}{R_{inv}} &= \{2(1-D)^2\pi^2 - 1 + 2\cos\phi_{inv}\cos(2\pi D + \phi_{inv}) \\ &- \cos 2(\pi D + \phi_{inv}[\cos(2\pi D) - \pi(1-D)\sin(2\pi D)])\} \\ &/\{4\sin(\pi D)\cos(\pi D + \phi_{inv})\sin(\pi D + \phi_{inv})\} \\ &[(1-D)\pi\cos(\pi D) + \sin(\pi D)]\} \end{aligned} \tag{18}$$

On the other hand, R_{inv} has another expression from the restriction of the class-E ZVS/ZDS conditions as

$$R_{inv} = \frac{2\sin^2(\pi D)\sin^2(\pi D + \phi_{inv}) V_D^2}{\pi^2 (1-D)^2 I_1^2 (R_{eq} + r_{L_1})}. \tag{19}$$

From (15) and (19), C_p can be obtained as

$$C_p = \frac{\omega L_{eq} R_{inv} \pm \sqrt{R_{inv}[R_{eq}^2(R_{eq} - R_{inv}) + \omega^2 R_{eq} L_{eq}^2]}}{\omega R_{inv}[R_{eq}^2 + \omega^2 L_{eq}^2]} \tag{20}$$

It is shown in (20) that there are two candidates of C_p. C_p for satisfying $L_0 = L_{inv} - L_x > 0$ should be selected because L_0 resonates with C_1. C_1 and C_S for satisfying the class-E ZVS/ZDS conditions are

$$C_1 = \frac{1}{\omega^2 L_0} = \frac{1}{\omega^2 (L_{inv} - L_x)} \tag{21}$$

and

$$\begin{aligned} C_S &= \frac{1}{\omega\pi^2(1-D)R_{inv}} \{2\sin(\pi D)\cos(\pi D + \phi_{inv}) \\ &\cdot \sin(\pi D + \phi_{inv})[(1-D)\pi\cos(\pi D) + \sin(\pi D)]\}. \end{aligned} \tag{22}$$

The dc-feed inductance L_C for ensuring less than 10 % current ripple of the input current is expressed as [12]

$$L_C = \frac{R_{inv}}{f}\left(\frac{2\pi^2}{4} + 1\right). \tag{23}$$

4. Design Example

4.1. Design Specifications

In this section, a design example of the proposed driver along with PSpice simulation results is shown. We consider to design a driver for the SiC MOSFET SCT2450KE. The gate capacitance and resistance were measured as C_g = 3 nF and R_g = 18.75 Ω. In addition, the amplitude of the gate voltage is specified as V_g = 15V because of the maximum gate voltage is 20 V. The design specifications of the proposed gate driver were given as operating frequency f = 7 MHz, dc-input voltage V_D = 20 V, on-duty ratio D = 0.5, and loaded quality factor of the secondary resonant circuit Q_2 = 3. Additionally, the specifications of the coupling coils are necessary. In this paper, loosely coupled coils are used to get leakage flux. We gave the coupling coefficient k = 0.2 and the ratio of the number of turns L_1/L_2 = 1.

4.2. Design Procedure

4.2.1. Secondary part design

From $Q_2 = 3$ and specified C_g and R_g, the secondary inductance and capacitance are fixed as $L_2 = 1.28\ \mu$H and $C_2 = 467$ pF, respectively. Therefore, we have $L_1 = 1.28\ \mu$H from $L_1/L_2 = 1$.

From $C_g = 3$ nF and $C_2 = 467$ pF, we have $C_r = 404$ pF. In addition, the amplitude of the secondary current can be obtained from (3) as $I_2 = 0.742$ A. Therefore, the amplitude of the input voltage of the rectifier should be $V_{ind} = 14.5$ V from (9). The equivalent inductance and resistance of the secondary part is obtained from (12) and (13) as $R_{eq} = 6.46\ \Omega$ and $L_{eq} = 1.28\ \mu$H, respectively.

4.2.2. Primary and coupling part designs

From (14), the amplitude of the output current of the inverter is $I_1 = 1.29$ A. From the above obtained values and (20), we have $C_p = 228$ pF. For satisfying the class-E ZVS/ZDS conditions, the capacitances should be $C_1 = 287$ pF and $C_S = 111$ pF from (21) and (22), respectively. Finally, the dc-feed inductance for ensuring less than 10% current ripple of the input current is expressed as $L_C > 37.3\ \mu$H. $L_C = 40\ \mu$H is used in the simulation.

4.3. Experiment and PSpice-Simulation Results

Figure 3 shows waveforms of the designed driver obtained from analytical expressions, PSpice simulation, and circuit experiment. It can be confirmed from Fig. 3 that the switch voltage of all results achieved the class-E ZVS/ZDS conditions and the specified amplitude of the drive voltage. In addition, it is also confirmed that the simulation and experimental waveforms agreed with the analytical waveforms quantitatively. It can be stated from these results that the analytical expressions and design procedure have sufficient validity for designs of the proposed driver.

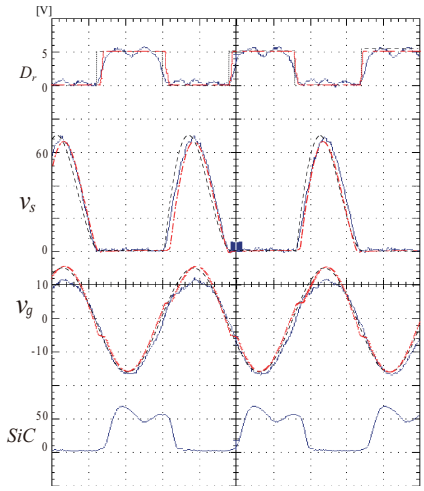

Figure 3: Waveforms of the designed driver obtained from the analytical expressions (solid line) and PSpice simulation (dotted line).

5. Conclusion

This paper has presented the isolated class-E driver for SiC MOSFETs along with its analysis and design procedure. The proposed driver achieves high power-conversion efficiency at high frequencies. The validity of the analytical expressions and design procedure were shown by the quantitative agreements of waveforms among analytical expressions, PSpice-simulation, and circuit experiment.

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