5.8 GHz Simple Compact Folded Dipole Rectenna without Chip Capacitor

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1. Introduction

The rectenna is an RF power receiver converting the received power into DC power that can then be consumed by other subsystem. Recently, the compact rectenna technology has gained great attention in many of the sensor applications [1, 2]. Designing of a rectenna system is difficult in matching the antenna impedance with that of the rectifying diode. Unlike the impedance matching for traditional antennas, the conjugate matching method is needed for designing the rectenna to get high power transmission between rectenna and diode. In most of the published literatures, a matching network was designed between the antenna and rectifying circuit which increased the system design complexity and also extended the total rectenna size or layers [3].

In this paper, a simple wideband folded dipole [4] is modified for rectenna system design. The diode is directly connected with the antenna saving the matching network. The required conjugate matching can be achieved by adjusting appropriate geometry parameters of the antenna. The proposed rectenna has a very compact size, uni-planar structure, and low cost. In addition, the lumped chip capacitor is also saved by the embedded edge gap capacitor effect to further save the system cost. A 5.8GHz rectenna is designed and measured to show this novel architecture.

2. Folded Dipole Rectenna Design

2.1 System Architecture

5.8 GHz is chosen as working frequency band. A wideband planar folded dipole with self-balanced impedance property is modified as the antenna. The proposed novel rectenna architecture is shown in Fig. 1. The diode is located in the middle of the bottom side of the rectenna. In the centre of the rectenna, two edge gaps replace the conventional chip capacitor. The coplanar strip line for connecting the load resistor has no observable effect to the antenna performance and thus it is just kept small enough. When the RF energy transfers to the rectenna, RF signal is received by the diode-loaded wideband folded dipole. The diode rectifies the RF energy received from antenna directly. From DC point of view, since DC signal cannot pass through the centre gap, the received RF energy would be delivered to the load resistor.

2.2 Diode Impedance Study

In this design, the large signal model of HSMS-2820 Schottky diode is used. Considering the limitation of the power of our power amplifier, 6 dBm received power is chosen for calculating the conjugate matching impedance of diode. Agilent Advanced Design System (ADS) is used in this step and the simulation setup is shown in Fig. 2. When the 6 dBm power adds to the diode, the perfect conjugate matching value can be obtained from optimization as shown in Fig. 3. In this situation, the diode impedance is 17.653+j31.312, and the port impedance is 17.653-j31.312.

2.3 Folded Dipole Rectenna Design and Simulation

To guarantee this simple architecture, a 5.8 GHz rectenna is designed and fabricated on the 0.5 mm thick Teflon substrate (dielectric constant = 2.55) with 0.018 mm copper cladding. 1 kΩ load resistor is chosen in this design. IE3D is used for design and final optimization. Based on the study [4], the value of W is related with antenna impedance in Fig. 3. To reach the required antenna input impedance, the value of W, L, and gap is optimized. The goal of the setup is for perfect conjugate matching. The antenna load impedance is set as 17.653+j31.312 which is the desired diode impedance. The input impedance of the antenna is optimized to reach 17.653-j31.312. The final optimized value is shown in the Fig. 3. Fig. 4 shows the frequency related with the conjugate matching factor. '1' means the perfect conjugate matching. In the desired 5.8 GHz, conjugate matching factor of 0.998873 is obtained. The antenna gain, S_{11}, and radiation pattern are shown in Figs. 5, 6, 7, respectively. The S_{11} is already renormalized to the port impedance 17.653+j31.312. From Fig. 6, based on the complex impedance of the antenna design, there is almost no second harmonic generated from the proposed antenna which simplified the system design consideration for second harmonic re-radiation from the rectenna system. A disadvantage is also observed. The centre gap reduces the antenna efficiency and only 0.52 dBi gain is obtained from the simulation result.

3. Experimental results

The fabricated 5.8 GHz rectenna and measurement setup are shown in Fig. 8 and Fig. 9, respectively. The measurement setup and conversion efficiency calculation are followed by the study [5]. The measurement distance is set as 1.2 m. To calculate the system efficiency, the proposed folded dipole antenna gain is needed. However, the proposed folded dipole antenna is not designed based on 50 ohm. Therefore, it is hard to measure the proposed antenna gain accurately in that situation. To calculate the conversion efficiency, the simulated gain is used. It should be pointed out that in conventional calculation of the rectenna conversion efficiency, the antenna with filter network is needed for the design and measurement without considering the load and the diode. Since the proposed rectenna gain is simulated including all the system components, it is a more systematic design method and very suitable for the first-pass system success. Table 1 shows the measured output voltage and the calculated conversion efficiency with three different load resistor values.

4. Conclusion

A simple architecture rectenna system has been developed. It has been shown that the proposed rectenna system simplifies the design work. In addition, the conventional chip capacitor is also saved by the edge gap capacitor effect, which further reduces the system cost whereas makes a lower antenna gain. The proposed rectenna has a compact size, uni-planar structure, and low cost. It is very easy to fabricate and connect to the other subsystem to supply the power. Considering the above advantages, this novel architecture rectenna system is very suitable for the small sensor applications.

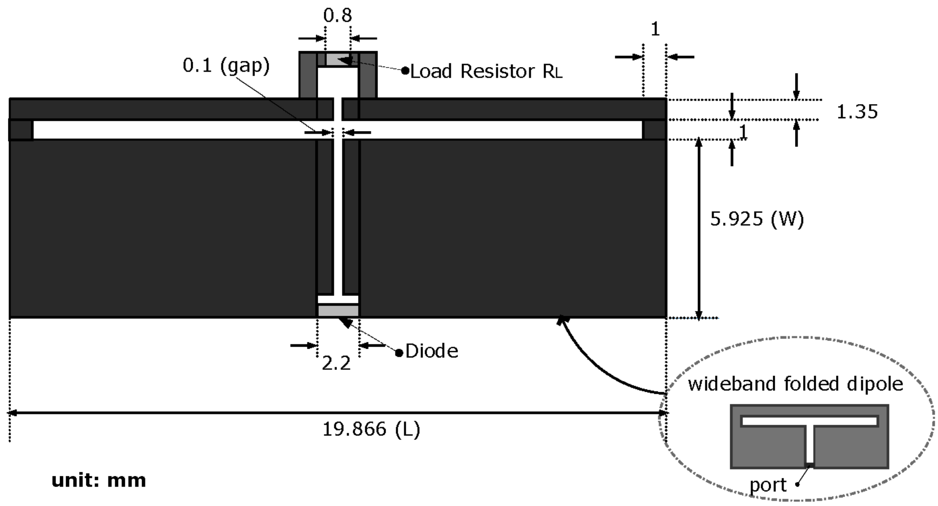
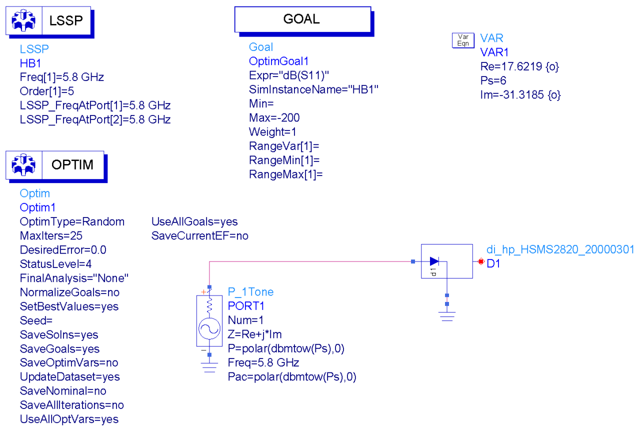


Figure 1: Geometry of the proposed folded dipole rectenna



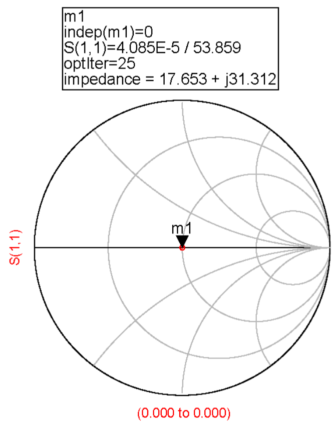
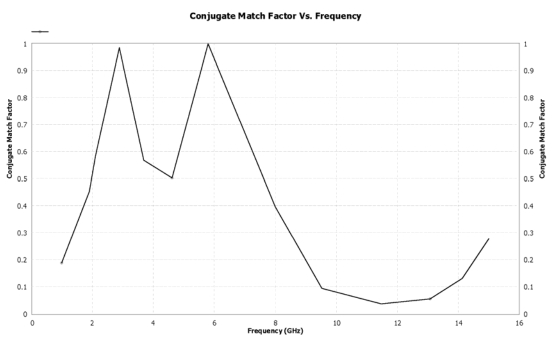


Figure 2: Diode conjugate matching impedance analysis   Figure 3: Impedance at matching point



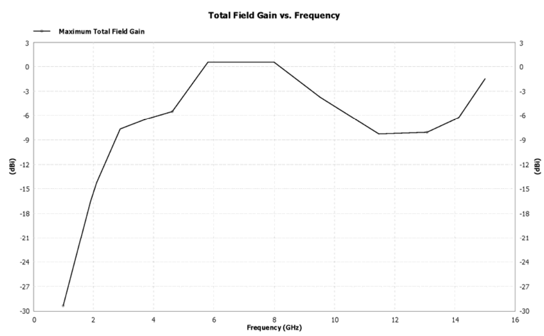


Figure 4: Conjugate matching factor   Figure 5: Gain of the rectenna

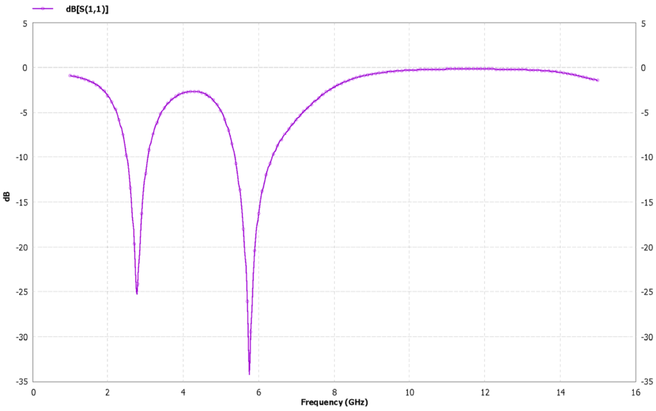


Figure 6: Return loss of the rectenna

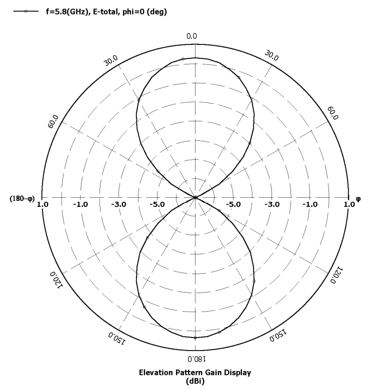


Figure 7: Radiation pattern of the rectenna

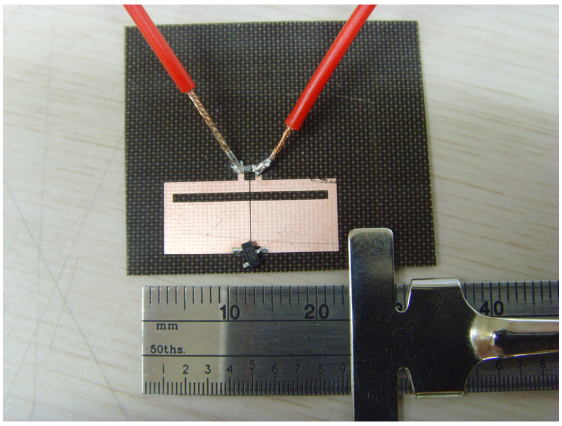


Figure 8: Photograph of the rectenna

Figure 9: Measurement Setup

Table 1: Output voltage and conversion efficiency with various load resistors

Load Resistor (ohm)	Output Voltage (volt)	Conversion Efficiency (%)
100	0.13	7.13
500	0.54	24.6
1000	1.1	51.1

References

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