11D3-2

Wide Temperature Range 1.25-Gb/s Burst-Mode Receiver Chip Set for G-PON Optical Receiver

Y. Tsunoda[*1], S. Ide[*1], T. Yamabana[*1], Y. Hattori[*2], S. Sakuramoto[*3], T. Matsuyama[*3], K. Mori[*1]

[*1] Fujitsu Laboratories Ltd. [*2]Fujitsu VLSI Ltd. [*3]Fujitsu Limited
Fujitsu Laboratories Ltd., 10-1 Morinosato-Wakamiya, Atsugi city, Kanagawa, 243-0197, Japan
tsunoda.yukito@jp.fujitsu.com

Abstract We developed a 1.25-Gb/s optical burst-mode receiver chip set with a new ATC stabilizing method, which supports a wide operating temperature range. This new ATC method suppresses sensitivity degradation and output waveform duty fluctuation and pattern jitter caused by fluctuations in the threshold level. Using this method, we achieved high sensitivity, a wide dynamic range, and a fast settling time over the full -40°C to 85°C temperature range. These performance results comply with the specifications defined in ITU-T Recommendation G.984.2 Class B+.

1. Introduction

Recently, the use of high-speed access networks for broadband communications has been spreading widely throughout the world. A passive optical network (PON) system is one of the most promising technologies to implement access networks because of its advantages in communication speed and cost. In particular, a gigabit-capable passive optical network (G-PON) that meets ITU-T Recommendation G984.2 [1] is demanded in North America because it is consistent with SONET/SDH systems.

For G-PON up-stream transmission, a 1.25-Gb/s burst-mode optical receiver is a key technology for high-speed decision threshold of the received packets, whose power varies widely due to different optical path lengths. An automatic threshold control (ATC) circuit is an optimal solution for a burst-mode receiver, which detects the threshold levels of the received packets using peak and bottom hold circuits. To reduce ATC settling time, it is necessary to use small hold capacitances in the peak/bottom detector.

However, if small hold capacitances are used, a fluctuation in the threshold level occurs, which is caused by leakage of electric charge. Threshold level fluctuation leads to changes in the duty ratio and pattern jitters of the output signals. In that case, it not only degrades the sensitivity but also makes it difficult for clock data recovery (CDR) circuits to recover the clock [2,3]. Because the leakage of charge occurs through the transistor, which is followed by small hold capacitance at high temperature, it is important to suppress threshold level fluctuation by this leak to achieve an optical receiver that operates in a wide temperature range.

In this paper, we developed a 1.25-Gb/s burst-mode optical receiver chip set using a new ATC method that suppresses the threshold level fluctuation to reduce the change in the duty ratio. Using this method, the pattern jitters were reduced, and a receiver that had this chip set achieved high sensitivity of -34.4 dBm and a wide dynamic range of over 30 dB over the full -40°C to 85°C temperature range.

2. Structure

Figure 1 depicts a block diagram of our burst-mode optical receiver. The optical receiver consists of a photodiode (PD), a transimpedance amplifier (TIA) with variable-transimpedance, and a burst-mode limiting amplifier with the ATC circuit.

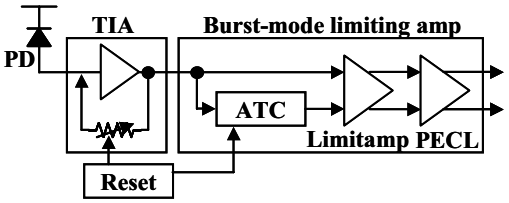


Fig. 1 Optical burst-mode receiver for optical line termination (OLT)

To reduce the threshold level fluctuation, we devised the "*ATC Stabilizer Method*" as shown in Figure 2. The ATC circuit, which consists of the peak hold circuit, bottom hold circuit, and a 1/2 circuit, detects the middle level of the signals as the threshold level during preamble time. The *ATC stabilizer* fixes the peak and bottom hold levels after detecting the preamble.

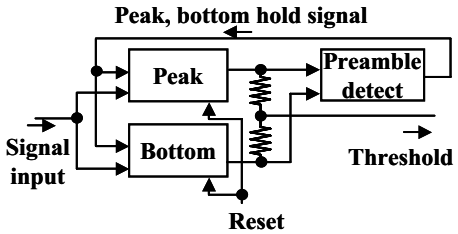
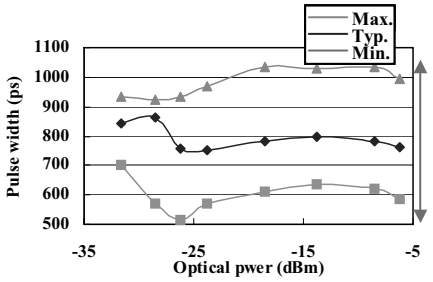


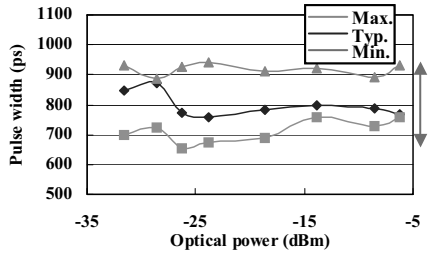
Fig. 2 ATC circuit block diagram with ATC stabilizer method

Figure 3 plots the simulation results of the pulse width of the output signals at 85°C, assuming a worst-case data stream with long successive 1's or 0's. As shown in Figure 3(a), the pulse width fluctuation of the output signals was ±300 ps when the *ATC Stabilizer* was not

used. However, the pulse width fluctuation of the output signals was reduced to ±150 ps when the *ATC Stabilizer* was used, as shown in Figure 3(b). This result indicates that the *ATC stabilizer* reduced the pulse width fluctuation by half.



(a) ATC stabilizer OFF



(b) ATC stabilizer ON

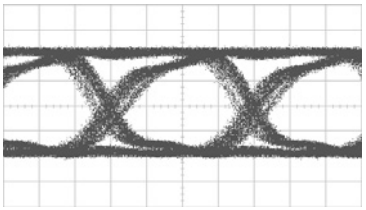
Fig. 3 Output waveform pulse width of receiver

3. Experimental Result

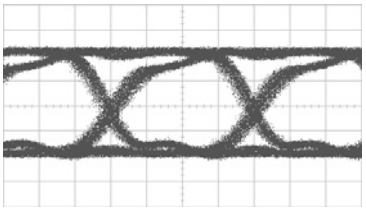
We developed this chip set using 0.18-μm standard CMOS technology in order to reduce the production costs.

We measured the output waveforms at 85°C to confirm the effect of the *ATC stabilizer*. An avalanche photodiode (APD) was used as the PD in this experiment to achieve high sensitivity. As Figure 4 shows, the output jitter was drastically reduced when the *ATC stabilizer* was used.

To investigate the performance of our burst-mode receiver, we evaluated the output waveform and the sensitivity for the case when a low power packet2 follows a high power packet1. Figure 5 shows the output waveform of the burst-mode signal. We achieved a fast settling time of a 5-bit preamble after the 32 bits, which is the minimum guard time between packets. Figure 6 plots bit-error rate (BER) measurements performed upon the pseudo random binary sequence (PRBS) part of the packets for the case when a low power packet2 follows a packet1 as high as -8 dBm. The receiver exhibited sensitivity of -34.4 dBm and overload of -4 dBm at a BER of 10^{-10} over the full -40°C to 85°C temperature range.



(a) ATC stabilizer OFF



(b) ATC stabilizer ON

Fig. 4 Output waveform of receiver

The burst-mode optical receiver with our developed chip set can support a wide operating temperature range, and has high sensitivity, a wide dynamic range, and fast settling time, resulting in a G-PON OLT receiver defined in ITU-T Recommendation G.984.2 Class B+.

4. Conclusion

We developed a 1.25-Gb/s burst-mode optical receiver chip set for G-PON OLT with an *ATC Stabilizer*. This chip set drastically reduced threshold level fluctuation and pattern jitter. The optical burst-mode receiver incorporating our chip set achieved high sensitivity and a wide dynamic range, which complies with specifications defined in ITU-T Recommendation G.984.2 Class B+, over a wide operating temperature range of -40°C to 85°C.

References

[1] ITU-T Recommendation G.984.2
[2] M. Sato, et al. Symposium on VLSI circuit digest of technical papers, 1998, 18.1
[3] H. Tagami, et al. J. of solid-state circuits vol. 41, No.11, 2006, pp. 2555-2565

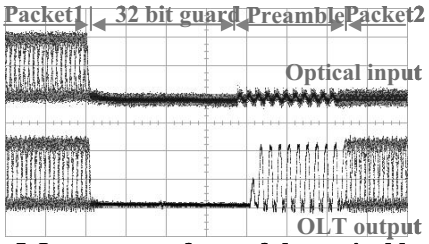


Fig. 5 Output waveform of the optical burst

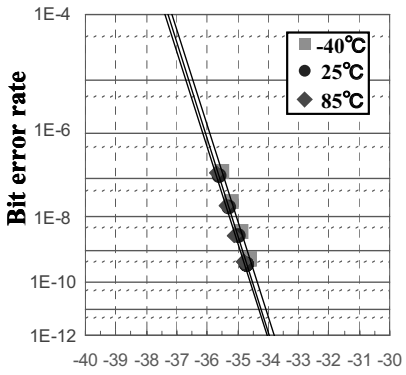


Fig. 6 BER measurement result