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Very Low Noise AlInAs Avalanche Photodiodes with Gain-Bandwidth product of 140 GHz

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Abstract:
We demonstrate a new planar junction AlInAs APD with carbon-doped charge layer achieving low dark current of 13nA (M=10) and very low excess noise factor of 3 (M=10). These characteristics are simultaneously achieved with a responsivity of 9.5 A/W (M=10) and a gain x bandwidth of 140 GHz.

Introduction:
Recent demand for high sensitivity receivers for 10Gb/s metro networks requires high performance avalanche photodiodes (APDs) because their internal gain improves sensitivity (>10dB) over traditional PIN photodiodes. In addition, avalanche photodiodes constitute a cost effective solution due to their compactness and low power consumption [1].
SAGM (Separate Absorption Grading and Multiplication) APD structures using bulk AlInAs avalanche material appear today as a good alternative to InP avalanche layer and achieve similar performances as AlInAs/AlGaInAs MQW APDs, the epitaxial growth of which is somehow more complicated [2], [3]. Owing to a high ionization coefficients ratio of 3-4, AlInAs APDs demonstrated a high gain-bandwidth product of 120 GHz and a receiver sensitivity of –29.8 dBm at 10Gb/s and BER of 10^{-9}, using either front or back illuminated structures [4], [5]. These results have been demonstrated using a simple mesa avalanche diode to define the absorption window which requires however an InP-regrowth step acting as a guard-ring layer to improve device reliability. Recently, a front-side illuminated APD has been realized using the well established planar junction technology using Zn-diffusion process and has demonstrated a low dark current of 160 nA at 0.9xVb (Vb is the breakdown voltage) and a gain-bandwidth product of 120 GHz [5]. However, as the diffusion process occurs at high temperatures (>500℃), a stable charge doping layer , which reduces the electric field in the absorption layer, is required.
In this paper, we report on a new planar junction AlInAs APD with carbon-doped charge layer. The flip-chip mounted APD primary responsivity reaches 0.95 A/W at 1.55 µm with a gain-bandwidth product of 140 GHz. The stability of the APD structure is displayed through a very low dark current figure with less than 20 nA dark current (at 0.9xVb) for avalanche gains up to 20. A very low excess noise factor of 3 at gain of 10 and an ionization coefficients ratio of 5-7 are additionally demonstrated.

APD Design and Fabrication:
The epitaxial structure of the SAGM APD is grown by MOVPE (Metallic Organo Vapor Phase Epitaxy) on an n-doped InP substrate. The vertical structure includes from the top an unintentionally doped InP window layer (1 µm) followed by an unintentionally doped InGaAs absorption layer (1.2 µm) and an unintentionally doped AlInAs avalanche layer (0.2 µm). An InGaAlAs grading layer (0.1 µm) is inserted between absorption and avalanche layers to avoid carriers trapping during transport between both layers. In addition, a stable and accurately defined charge doping layer made of C-AlInAs ($4x10^{12}$ cm^{-2}) is used to avoid high electric field in the absorption layer.
The process flow of our back-side illuminated APDs fabrication is made using optical lithography and is mainly based on dry etching process for mesa realization. Highly reliable planar junction is carried out by Zn diffusion to obtain p-InP region in the undoped InP window layer. This operation is made in an MOVPE reactor using DMZn as source doping material to improve process control by immediate switch on-off of doping gas and uniformity by substrate rotation. A PtAu and a TiPtAu layers which are patterned using lift-off are used for P- and N-contacts, respectively. After wafer thinning and anti-reflection coating on the back-side of the wafer, the APDs are diced and mounted using flip-chip on a high frequency carrier.
Figure 1 shows the equipotential lines calculated using a drift diffusion model. The simulation demonstrates a gradual evolution of the potential at the periphery of the junction as well as in the avalanche layer which avoids possible edge breakdown.

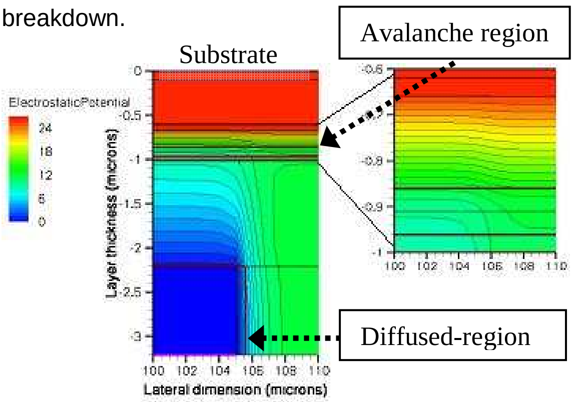

Fig.1: Equipotential lines simulation of the APD (starting from the substrate).

AlInAs APD Photodiode characteristics:

Figure 2 shows typical dark current, photocurrent and multiplication gain versus reverse bias voltage characteristics for a 30 µm diameter flip-chip mounted APD. The dark current remains low and stable (~ 10 nA) over a wide range of applied bias (from punchthrough 11-12 V up to gain M=10) and is less than 30 nA for avalanche multiplication factors of 30. This low dark current characteristics even at high avalanche gain indicates the good passivation process of the planar junction as well as the excellent stability of electric field distribution along the structure achieved using our newly developed Carbon-doped field control layer (charge layer). A high primary responsivity of 0.95 A/W is measured at 1.55 µm owing to the flip-chip assembly with no additional parasitic capacitances (depletion capacitance of 140 fF). The breakdown voltage is around 32 V allowing possible available multiplication gain of >100.

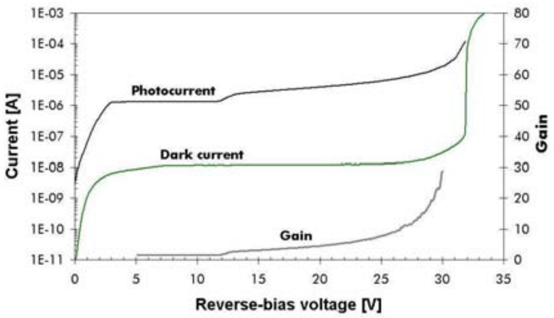

Fig.2: APD dark current, photocurrent and gain characteristics versus reverse bias voltage

Figure 3 shows the excess noise factor versus multiplication gain deduced from the noise spectral density measurements. Very low excess noise factors of 3 at M=10 are deduced corresponding to an ionization coefficient ratio k=5-7 (Teich model [6]).

The frequency response of the fabricated APD was measured from 130 MHz to 20 GHz at 1.55 µm. The bandwidth (3-dB) dependence on multiplication factor is displayed in Figure 4 where a gain-bandwidth (G.B) product of 140 GHz is achieved allowing a large maximum achievable gain at 10 Gb/s operation. This is to our knowledge the first time that a back-side illuminated APD displays such a large G.B product together with a primary responsivity of 0.95 A/W (M=1) and a low noise and dark current. In addition, to illustrate systems benefit of the new AlInAs APD for 10 Gb/s operation, calculations have been conducted on two avalanche receivers (TIA equivalent input noise is 16 pA/(Hz)$^{1/2}$): the first APD is characterized with an ionization ratio (k) of 3.3 and a dark current (Idark) of 1 µA (as shown on InP-APD) and the second (similar to the present new APD) with a k of 5.3 and Idark of 0.01 µA. A clear improvement (~ 2.5 dB) of the minimum received power is achieved at 10 Gb/s using a the later APD with a calculated sensitivity of – 32 dBm.

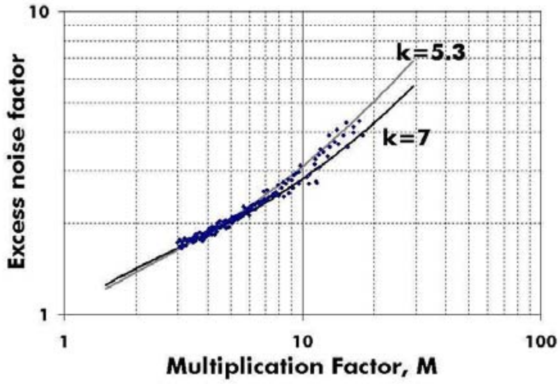

Fig.3: Excess noise factor vs multiplication factor (Teich noise model displayed for determination of k)

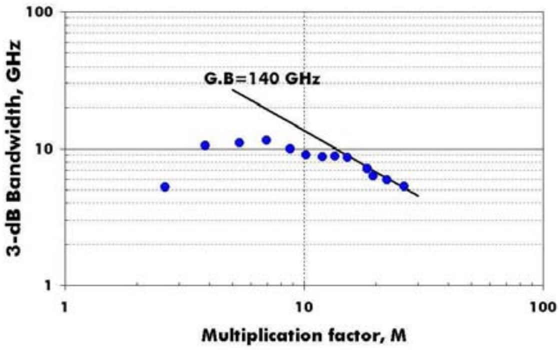

Fig.4: Frequency response versus multiplication factor of a 30µm AlInAs APD

Conclusions

A flip-chip back-illuminated AlInAs APD with a planar junction is proposed. Accurate control of the charge layer allows to achieve very low dark current even at high multiplication gain (Idark < 30 nA for M=30) and a multiplication process that is strictly concentrated in the AlInAs avalanche layer without unwanted multiplication in InGaAs absorption layer. Therefore a high ionization coefficients ratio of 5-7 is deduced from noise measurements (F=3 at M=10). High primary responsivity of 0.95 A/W at 1.55 µm was achieved on a 30 µm diameter APD together with a G.B of 140 GHz. These performances associated to a robust planar junction technology make those C-AlInAs APDs the choice candidates for 10 Gb/s receivers.

References

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