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Electronic mitigation techniques for 40 Gbit/s optical fiber transmission systems

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Abstract
Different aspects of electronic distortion equalization (EDE) at 40Gbit/s are highlighted: from the experimental assessment of the adaptation of analog equalizer circuits, over the numerical simulation of digital MLSE for spectrally narrowed transmission channels, to the estimation of the digital processing (DSP) effort in various schemes.

Introduction
Today's upgrade scenario for existing 10Gb/s WDM transmission links presumes a gradual replacement of 10Gb/s terminal equipment by 40Gb/s line cards while keeping the optical path designed for 10Gb/s operation, i.e. parameters and tolerances such as optical bandwidth given by WDM mux/demux for 100GHz or even 50GHz channel spacing, residual chromatic dispersion (e.g. up to 50km SMF) and PMD (e.g. up to 8ps). This demands robustness and distortion tolerance of the 40Gb/s transmission equipment. Today this is met by optical dispersion compensators (tunable grating CFBG) and optical PMD compensator. With the sustaining efforts to reduce size and complexity in future releases of 40Gb/s receiver boards, analog or digital (DSP) electronic signal processing schemes are investigated for electronic distortion equalization (EDE).

Adaptive analog distortion equalization
Lab devices of analog operating feed forward (FFE) and decision feedback equalizer (DFE) in SiGe or InP HBT technology have been realized and tested for 40Gb/s EDE application [1-3]. Though these devices of typically 5 forward taps and 1 feedback tap increase the tolerance of the system to many kinds of distortions by only some tens of percent, this might already be sufficient for links whose parameters are not so far away from 40Gb/s requirements.
For automatic adaptation of the equalizer consecutive dithering of the FFE taps are commonly used. The FEC error count provided by an FEC circuit might serve as feedback signal. The adaptation speed is mainly determined by the error rate since each dither step must wait for the collection of a sufficiently high number of errors (e.g. 1000) in order to obtain a stable (noiseless) feedback signal. With a BER around 10^{-4}, an update of the feedback signal can be expected within a few milliseconds.
Alternatively also an eye monitor can be incorporated which provides a parameter which is related to the eye opening or the Q-factor of the eye diagram of the equalized signal. For eye monitoring at 40Gb/s a novel IC has been fabricated in a preproduction state-of-the-art SiGe bipolar technology with two independently operating decision gates for data decision and monitoring, respectively. Opposite to FEC error count the eye monitor gate can inspect the eye closer to the rails at higher BER around 10^{-2}. Thus a sufficient number of errors can be collected in a shorter time enabling an approximately 100 times faster adaptation speed.

In the following experiment the reduction of the number of the automatically adapted taps of a 5 tap FFE has been investigated. The error count served as feedback signal. A 42.7Gb/s ASK-NRZ signal was distorted by a tunable DGD emulator. First the 1st and 5th tap have been optimised at 0ps DGD and then only the remaining three centre taps have been automatically adapted to the actual distortion (blue boxes in Fig. 1). In a further experiment the first three taps were automatically adapted and the last two were fixed (red triangles). Finally all 5 taps were adjusted (green dots). Fig. 1 exhibits that there is no difference visible between 3 and 5 adapted taps up to a DGD of 15 ps. This behaviour can be used to reduce the adaptation time.

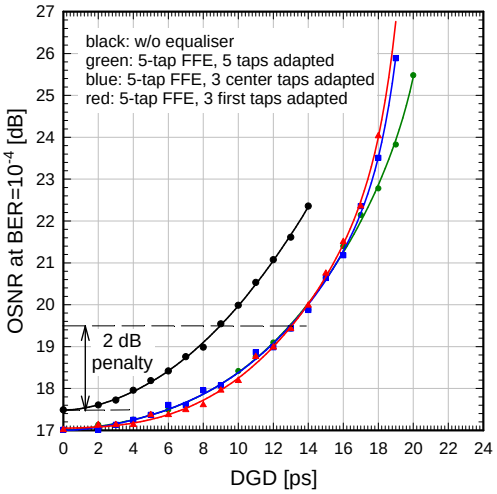

Fig. 1: Comparison of 5-tap FFE with 3 and 5 automatically adapted taps

Digital signal processing (DSP)
Complex digital 10Gb/s equalizers such as the maximum likelihood sequence estimator (MLSE) are already introduced as product. These MLSEs are suitable for distortion corresponding to an inter-symbol-interference (ISI) of up to 3 bits (4 state MLSE) [4] or 5 bits (16 states). In a numerical simulation (Monte-Carlo sim. for noise, BER = 10^{-4}) we compared the CD tolerance of an MLSE (4 states) in optical bandwidth limited channels. Fig. 2 shows the tolerance vs. optical filter bandwidth without equalizer (solid, RX) and with equalizer (dashed, MLSE) for the two modulation formats NRZ ASK and DPSK, respectively.
It is obvious that in the range of filter bandwidths of 50GHz down to 30GHz as they might be seen in (R)OADM cascades or in a 50GHz channel grid, the MLSE helps to keep the CD tolerance high.

Beside performance assessment based on dispersion or PMD tolerance analysis, in some presentations the realization constraints are already discussed by analyzing the penalty introduced by a finite analog-to-digital converter (ADC) resolution. But so far little attention has been paid to the complexity of the DSP processor itself.

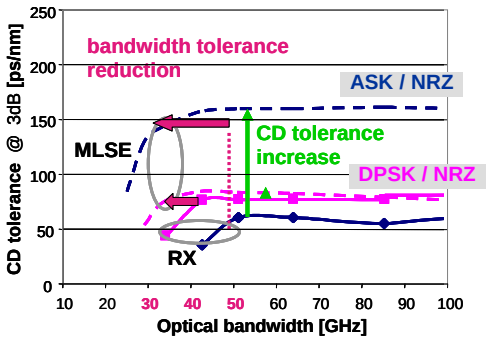

Fig. 2: Simulated chrom. dispersion tolerance vs. optical bandwidth for ASK (blue) and DPSK (purple) with MLSE (dashed lines) and w/o. equalizer (solid lines).

Here we introduce the parameter "Operations per bit-period T" (OpT) which quantifies the average number of calculation (real addition, multiplication, or metric extraction by RAM look-up table) applied to the digitized signal samples within the DSP processor. Further processing for adaptation, carrier or phase recovery as well as demultiplexing are not considered here. In the following we will discuss the processing effort of different DSP schemes for 1000 ps/nm dispersion compensation (60 km standard SMF).

The first DSP scheme we are looking at is the electronic pre-compensation [6]. It is based on an optical field synthesizer with electrical DSP calculation of the complex transmitter field. After digital-to-analog conversion (DAC) the electrical representatives of I and Q field components are converted into the optical domain by an external modulator. The inter symbol interference (ISI) of roughly 32 bits induced by 1000 ps/nm necessitates two FIR filters with 65 tap leading to 516 OpT (65 tap weight multiplications and 64 additions per filter and per half bit).
The core operation of the MLSE is concentrated the add-compare-select (ACS) unit which is positioned at each state of the trellis and governs 7 numerical operations per T. An extrapolation of 10Gbit/s simulations [7] to 40Gbit/s indicates that at least 4096 states are needed leading to a high processing effort of 28000 OpT.

The coherent detection scheme also referred to as intradyne detection, can be considered as the ultimate equalizer solution since it maps the phase and polarization information of the signal completely into the electrical domain [8,9]. If no further PMD compensation is applied and only one optical hybrid for phase diversity with two ADCs is realized, a complex 65 tap FIR filter processing the I and the Q signal samples is sufficient. It can further be reduced to 2 real 65 tap FIRs whose summation points are added, leading to 517 OpT, the same value as for the pre-compensation.

Optical OFDM [10,11] relies on fixed electronic DSP processing in both transmitter and receiver by fast and efficient realization of (inverse) Fourier transformers (IFFT/FFT) circuits and parallel but very simple adaptive processing of the individual subcarriers at the FFT output of the OFDM receiver. For a coarse DSP complexity assessment we determine the number of operations within the FFT and IFFT processor only. When spitting the 40Gb/s signal among 128 binary OFDM subcarriers the OFDM symbol has a length of roughly 3 ns. The IFFT processor at the transmitter with N=256 input samples (half of which are 0) provide a complex output signal for the I-Q modulator. An (I)FFT radix-2-algorithm requires about 5N log2(N) real numerical operations per OFDM symbol (3 ns) in both transmitter and receiver, which finally leads to 160 OpT.

All the operations per bit-period are summarized in the table Tab. 1. It is obvious that with 28000 OpT a MLSE for the distortion of 1000 ps/nm might be out of scope for realization. On the other hand optical OFDM with 160 OpT appears to be comparable to 16 state MLSE with the difference, that the processing is split among transmitter (IFFT) and receiver (FFT). Also electronic precompensation and intradyne detection are comparable from the signal processing effort (517 OpT).

DSP @ 40Gb/s	ops/T: **OpT**	**CD** @40Gb/s
MLSE 16 states	150	±200ps/nm
El. precompensation 2x65t. FIR	517	±1000ps/nm
MLSE 4096 states	28000	
Intradyne equalizer 2x65t. FIR	517	
Opt. OFDM, Ts=3ns (IFFT+FFT)	160	

Tab. 1: DSP processing effort (pure equalization effort) of different DSP-based equalization schemes.: Operations per bit period (T) for CD mitigation at 40 Gb/s.

Conclusion

At 40Gitb/s electronic distortion equalization performance and adaptation dynamics of analog electronic equalizer circuits are already investigated in lab experiments. Due to the higher complexity various kinds of DSP based equalization schemes are in the infancy for 40Gbit/s application ranging from MLSE to intradyne equalization. Numerical evaluation indicates that the MLSE facilitates or even enables transmission at high distortion tolerances even over existing 10Gb/s infrastructure (WDM filters) with low bandwidth (e.g. ROADM cascade). For the assessment of DSP signal processing complexity the parameter "operations per bit-period" (OpT) has been introduced and applied to chromatic dispersion mitigation (1000ps/nm). Optical OFDM has the potential of the least complexity, followed by intradyne detection and electronic pre-compensation. MLSE is more than two orders of magnitude more complex.

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