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Design and Implementation of a Routing Protocol for Power Packet Network

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Abstract– In this paper, we study the routing protocol for power packet networks. In the conventional routing protocol, since the router needs to read all header information before forwarding packet to other routers, the network might suffer high latency when the networks size is increased. We proposed the new protocol to reduce the processing time for routing at the router. In our proposed protocol, the router does not need to read entire header information for forwarding packet. Therefore, the processing time of the router is reduced. We implement the proposed protocol on a micro-computer board, which can be used as a controller of the power packet router. The simulation results show that our proposed protocol can not only properly operate in power packet networks but also provide lower latency than the conventional routing protocol.

1. Introduction

In recent years, as a new application area of the wide band gap semiconductor, small integrated circuit that is switchable on high voltage and high frequency is under developing by using power device like SiC or GaN. It is expected to transmit energy in packets. The power packet network that enables energy transfer [1] by the power packets has been developed in Ref. [2]. The sources transfer power packets to arbitrary load via power packet routers.

In this paper, we design the routing protocol for power packet network. Further, we implement the proposed protocol on a micro-computer board as a controller of the power packet router, and verify its operation. In conventional protocol, each router needs to read all header information before forwarding packet. This might lead to the increasing of the delay when the networks size is increasing. Furthermore, it is difficult to directly apply routing protocols in communication networks for transmitting power packet, because the bit rate on the power packet network is significantly slow compared to the communication networks. Therefore, it is necessary to develop low-latency protocol at a low bitrate.

We design the protocol for power packet routing with low delay. Our protocol is based on the protocol in the layer 2 of the OSI reference model (data link layer). To validate the operation of the networks, we implement the proposed protocol on a micro-computer board as a controller of the power packet router.

2. Design of the protocol in power packet routing

In this paper, we design the protocol for the power packet router developed in [2]. The power packet delivers electric power according to the attached information (such as the destination address) superimposed on the voltage waveform. A schematic diagram of a power packet router developed in the literature [2] is shown in Fig. 1. When the power packet comes to the router, the header information will pass through isolator to the controller. Based on the destination address in the header, the controller orders the gate driver to forward power packet to the destination. The gate driver controls the switch circuit to send the power packet via output port. Finally, the power packet router attaches the header information based on the original one stored in the memory.

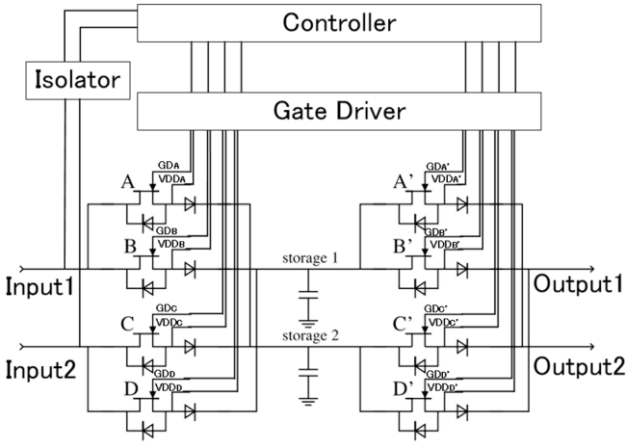

Fig 1: Schematic diagram of power packet router. [2]

In the routing algorithm in the literature [2], after reading the entire header information, the router checks the destination address in the header and their own routing table. Then, the router determines the destination port and forwards a packet. For example, in Fig.2, after reading all information about the destination address (DA) and source address (SA) and checking with routing table, the router will forward packet to destination router via corresponding port. However, as the increasing of network size, the header length becomes longer and the router takes more time to read the information. The power packet network might suffer high latency.

Therefore, we design the routing protocol referred to TRILL (Transparent Interconnection of Lots of Links)

standardized in RFC6325 [3] and RFC6326 [4] by IETF, to provide a low-latency routing. This routing protocol operates at layer 2 of the OSI reference model (data link layer), and forwards the packet efficiently by implementing in the inter-router communication.

As shown in Fig. 3, we add an identifier that includes destination router identification (DR) and source router identification (SR) for the router before the destination and source address information. The number of identifier for the router is much shorter than the number of individual addresses assigned to all routers in the network. Therefore, in the inter-router communication, the router starts to forward packet immediately after reading the router identifier of the header and checking the DR and the routing table. In our proposed protocol, because the router does not need to read entire header information for forwarding packet, the processing time at the controller in the router is small. Therefore, our protocol protocol can reduce the latency of the networks, especially when the number of router in network is large.

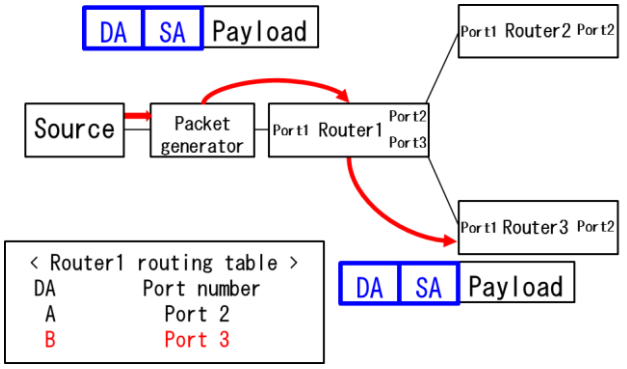

Fig 2: Routing method of existing power packet router.

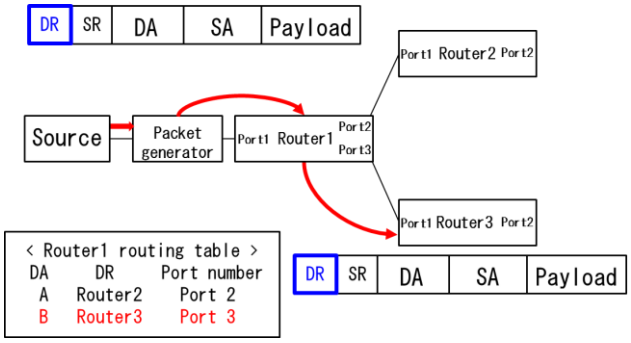

Fig 3: Proposed routing method in this paper.

3. Implementation of the protocol for power packet routing

We implement the proposed protocol in an open source hardware Arduino, which can be used as a controller of the power packet router. We validate the proposed protocol and compare the performance with a simple conventional protocol.

3.1. Prototype format of the protocol for power packet routing

In carrying out the implementation of the protocol for power packet routing, we propose a prototype format of the power packet referred to the OSI reference model and TRILL in Fig 4.

First, we add the preamble 12 bits for synchronization to the top. The following 8 bits are dedicated for the source and destination router ID (each 4 bits), which cover for 16 routers. The following 3 bits are indicated the QoS (Quality of Service) that corresponds to ToS (Type of Service) in IP. These bits are used for implementing priority control and bandwidth control. The following 16 bits are the destination address and the source address (each 8 bits), which cover 256 loads. Finally, three bits are used for Type to indicate the protocols such as IPv4 or IPv6 in the upper layer.

3.2. Network configuration in the experimental environment

We setup the experimental environment as in Fig. 5. Our power packet network includes one source, 4 routers to forward the packet. We use three different LED lights as the load in the experiment. The bit rate is set to 20 Hz, the packet transmission interval is set to 3 seconds, and the packet format is as shown in Fig. 4.

As operation check, we assign different addresses to red, yellow and blue LED lights, and transmit the power packet from source. We measure the voltage at the router with oscilloscope to confirm that the router starts to transmit the power packet immediately after reading the DR in the header.

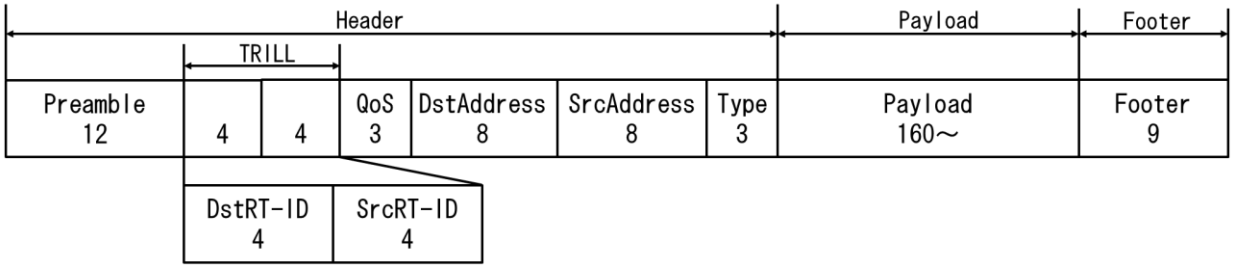

Fig 4: A format of the power packet routing protocol used in the implementation.

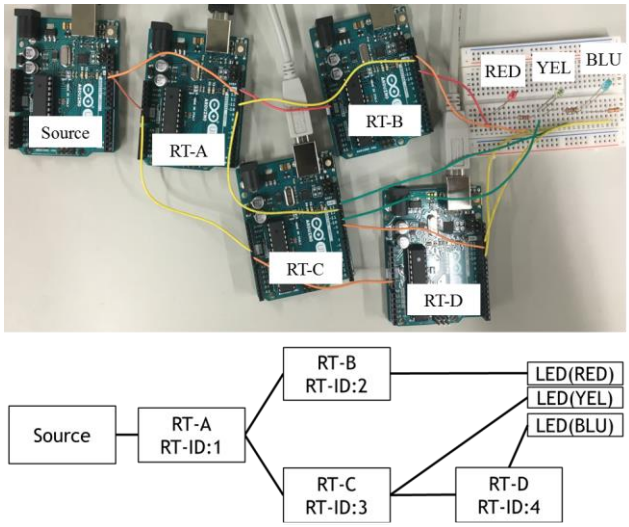

Fig 5: Experimental environment and network configuration diagram.

3.3. Experiments on proposed routing protocol

3.3.1. Waveform at transmitting the packet to red LED

Fig. 6 shows the waveform of the transmitting packet from RT-A to red LED. The points 1, 2, 3 in Fig. 6 are the observation points. The waveforms of observation points 1 and 2 show that the packet is started to transmit immediately after reading the destination router ID.

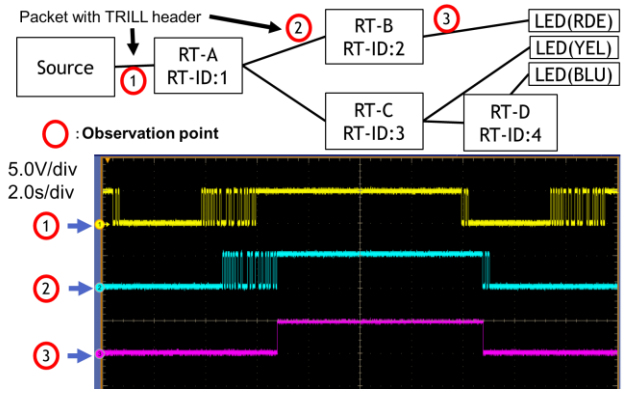

Fig 6: Waveform at transmitting the packet to red LED.

3.3.2. Waveform at transmitting the packet to yellow LED

Fig. 7 shows the waveform of the transmitting packet from RT-A to yellow LED. The waveform of observation points 1 and 2 show that the packet is started to transmit immediately after reading the destination router ID.

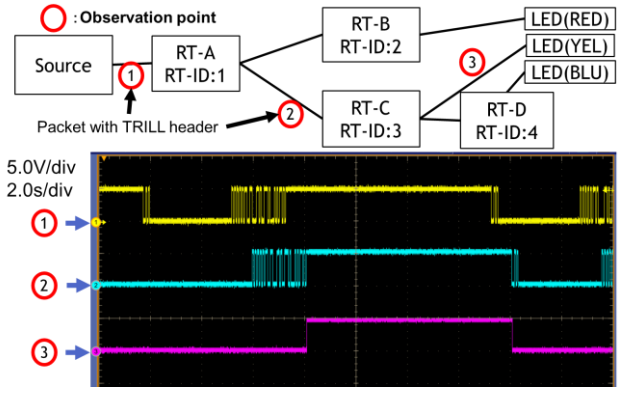

Fig 7: Waveform at transmitting the packet to yellow LED.

3.3.3. Waveform at transmitting the packet to blue LED

Fig. 8 shows the waveform of the transmitting packet from RT-A, RT-C, RT-D to red LED. The points 1 to 4 in Fig. 8 are the observation points of the power packet. Although in this route, we transmit the packet over longer path than the previous, the packet is also started to transmit immediately after reading the destination router ID.

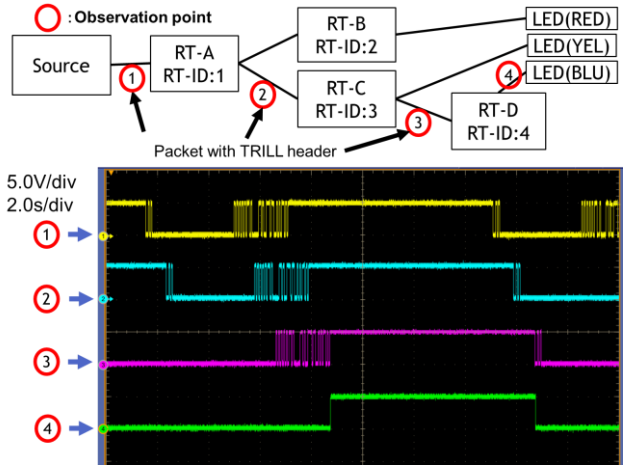

Fig 8: Waveform at transmitting the packet to blue LED

3.4. Comparison of the waveforms in the conventional method and the proposed method

We also implement the conventional method on Arduino for comparison. In the conventional method, we use the packet format which is removed the destination router ID and the source router ID from the packet format of Fig. 4. On this setting, we observe the waveform at transmitting the packet to blue LED, and compare two methods. Fig. 9 shows the waveform of the conventional method and the proposed method. And the waveform of the proposed method is same as Fig 8.

From the comparison of the two waveforms shown as in Fig. 9, the proposed header is 8 bits longer than the

conventional method, however the time until the power reaches the red LED is shorter than the conventional one. That is because the processing time of the router in our proposed protocol is reduced.

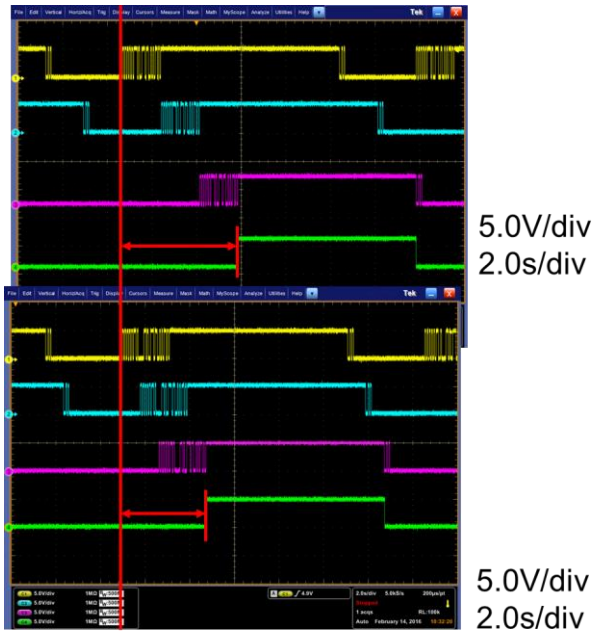

Fig 9: Comparison of the waveform in conventional method and proposed method.

4. Conclusion

In this paper, we designed and implemented a routing protocol for the power packet networks. In order to reduce the processing time at each router, we designed a routing protocol based on TRILL. Since each router starts to transmit power packet immediately after reading the DR in the header, our proposed protocol provides low latency for the networks.

By implementing the proposed protocol, we confirmed that our proposed protocol can operate properly in current designed power packet networks. Furthermore, we also achieve lower latency than the conventional method.

In this paper, we have implemented the controller part for verifying the operation of the proposed protocol. Currently, we are trying to implement the proposed protocol on a power packet router system.

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