Design of Circularly Polarized Patch Antennas with Coaxial Feed through a Silicon Chip

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1. Introduction

In late years, semiconductor devices have increasing demands for smaller size and more functionality as the radiator. In order to meet these demands, 60 GHz millimeter wave antenna integrated in silicon CMOS chip has very attractive features that offer massive available bandwidth and high-speed. A bottleneck of the antenna design is that the substrate thickness is too thin (~10 μm) to realize high efficiency and/or wide bandwidth. So, the antenna structure on the back side of silicon CMOS chip with a thick resin (~200 μm) had been proposed by the authors [1].

A dipole antenna on the backside of a 60 GHz silicon CMOS chip has been investigated [1]. The dipole antenna is on thick resin with about 200 μm to achieve high radiation efficiency and bandwidth on the backside of a 5mm square silicon CMOS chip in 60 GHz band. The dipole antenna is connected through via hole to the RF circuit layer on the opposite side of the same CMOS chip. The antenna was fabricated on the resin and the reflection, the gain and the radiation pattern were measured by using the waveguide aperture feeder which is not realistic. In this paper, the coaxial feeder through the resin on the backside of chip is designed for a circularly polarized 2x2 patch antenna array for monopulse operation as shown in Fig.1. The challenge here is that not only four radiating element but also their coaxial feeders should be accommodated in a very small and limited space of the 5mm square chip. The monopulse operation gives a simple method to find the direction of arrival, and the circular polarization dispenses with polarization adjustment between transmission and received antennas. Sequentially rotated arrangements [2] for the 2x2 array element are used, as shown in Fig. 1 (b) to gather via holes near the center of the chip. The sequentially rotated arrays arranged with quadrature phase excitation of 0°, 90°, 180°, 270° would be achieve by using the RF circuitry on the backside of the chip.

2. Antenna Design and Consideration

Fig. 2(a) shows a single radiating element which is a square patch antennas with the edge trimmed off. The patch antenna is placed on a 5mm square thick resin with dielectric constant of 2.84, loss tangent 0.015 and thickness 200μm. Firstly, linearly polarized square patch antenna is designed as shown in Fig. 2 (a). The length of the patch antenna is found to be a=1.28 mm at design frequency 62.5 GHz for the lowest return loss for impedance matching. The square patch antenna is then transformed into circularly polarized antenna by degeneracy separation method. Two diagonal corners of a square patch are trimmed off. The dimension of w=0.2 mm is determined to lower axial ratio below 1 dB. Next, 2x2 patch antenna array elements are placed as shown in Fig. 1. Fig. 1 (a) shows regular arrangement, while Fig. 1 (b) shows sequentially rotated arrangement to reduce space for via holes on the RF circuitry. The orientation of the patch antennas are arranged sequentially in 0°, 90°, 180°, 270°. This arrangement is to prepare for future fabrication where the quadrature phase excitation will be obtained by using the output from the RF circuitry on the CMOS chip

The patch antennas are fed by quasi coaxial cables with characteristic impedance of 50 Ohms. The distance between two center points of two radiating elements, D is fixed to be a half wavelength (2.4 mm). A FEM-based 3D full wave EM solver, Ansoft HFSS, is used for design. The cross sectional view of simulation analysis model is shown in Fig. 2(b). The inner and outer diameters of 0.2mm and 0.4mm respectively, are used in the simulation.

3. Results

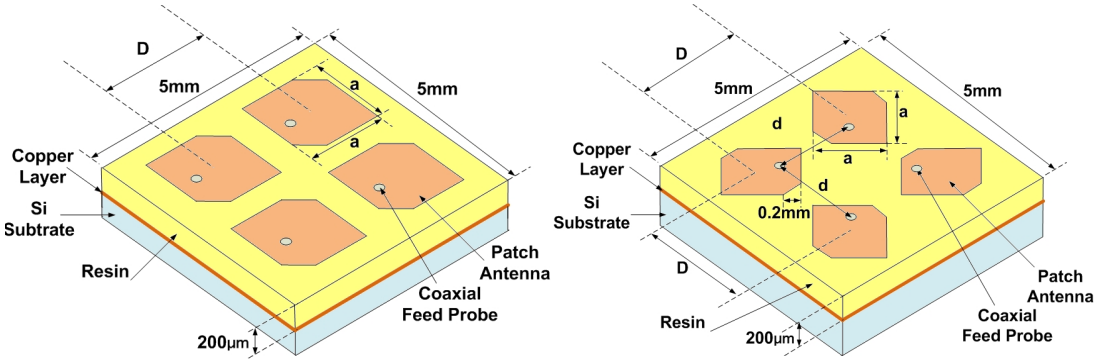
Fig. 3 shows the axial ratio by varying length *w*. It is found that the axial ratio is lowest for *w* = 0.2mm. Fig. 4 shows the frequency characteristic of axial ratio and reflection. Figure 4(a) shows the frequency characteristic of the axial ratio at boresight. The axial ratio for sequential array is very small independent of frequencies, in principle, since the ideal quadratic phase is assumed for the excitation. Fig. 4(b) shows the relative bandwidth of the array with sequential arrangement is 9.6 % for S_{11}<-10 dB. It has a wider bandwidth than the regular arrangement. By fixing the element spacing *D* at 0.5 wavelengths(2.4 mm), the optimized distance where VSWR is lower than 2 for return loss, the distance between two feed probes *d* between two radiating element is found to be 0.4 wavelengths as shown in Fig. 5. In Fig. 6(a), it shows that axial ratio for conductor diameter is below 1dB. From Fig. 6(b) it is found that the return loss is around -16dB, the bandwidth for VSWR wave ratio less than 2 designed at center frequency 62.5 GHz are found to be 8.4 %. Fig. 7 shows the summation (Σ) and difference (Δ) gain characteristic for monopulse operation. It shows a null depth of more than 30dB for the difference pattern, side lobe level lower than -20 dB for the sum pattern, calculated radiation efficiency to be 82.2 %.

4. Conclusion

We have proposed a circularly polarized 2x2 patch array for monopulse operation on a backside of a 5 mm square silicon CMOS chip in 60GHz. The simulation results show that this antenna provides good circular polarization and also low VSWR. It was shown that the sequentially rotated 2x2 patch array antenna have relative bandwidth of 9.6% for S_{11}<-10dB, axial ratio less than 1 dB and radiation efficiency of 82.2%. The future work is to fabricate the prototype and comparing measurement results with the simulation results.

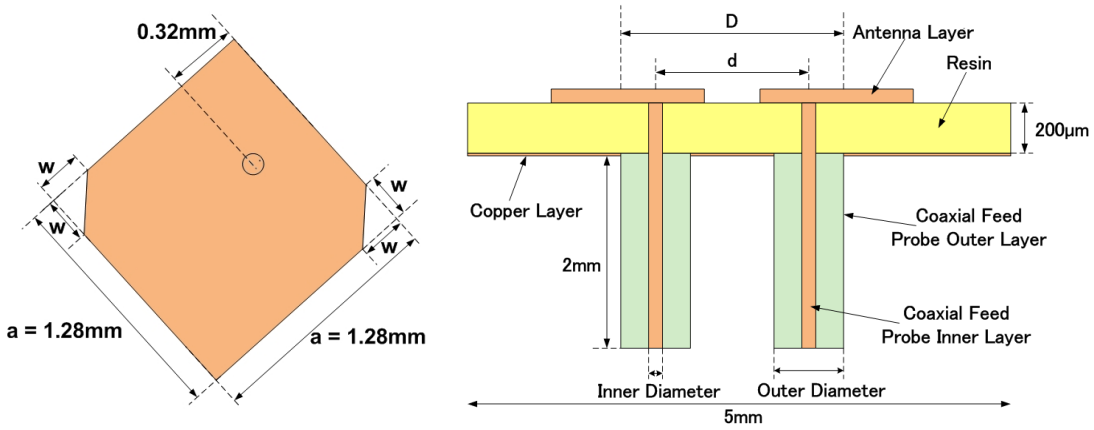
Acknowledgments

This work was partly supported by “The research and development project for expansion of radio spectrum resources” of The Ministry of Internal Affairs and Communications, Japan.



(a) Regular Arrangement (b) Sequentially Rotated Arrangement

Figure 1: 2x2 Patch Antenna Arrays on the Backside of a Silicon CMOS Chip



(a) Patch Antenna Element (b) Cross sectional View

Figure 2: Analysis Model

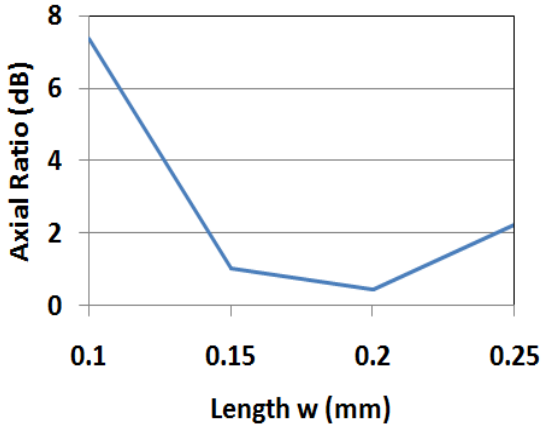
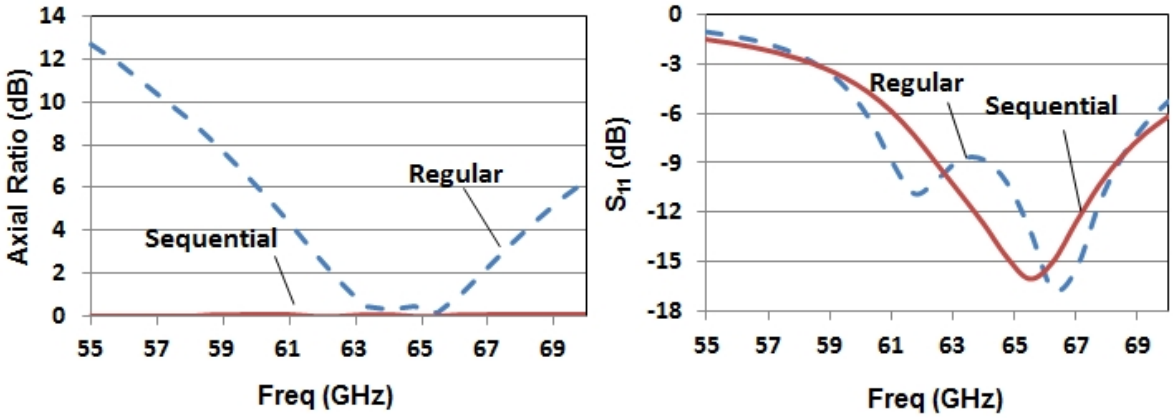


Figure 3: Axial Ratio to determine length *w*



(a) Axial ratio (b) Return Loss

Figure 4: Axial ratio and return loss for 2x2 element array in regular and sequential arrangement.

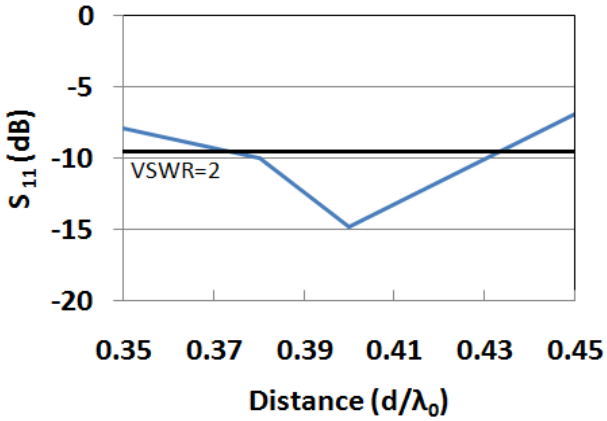
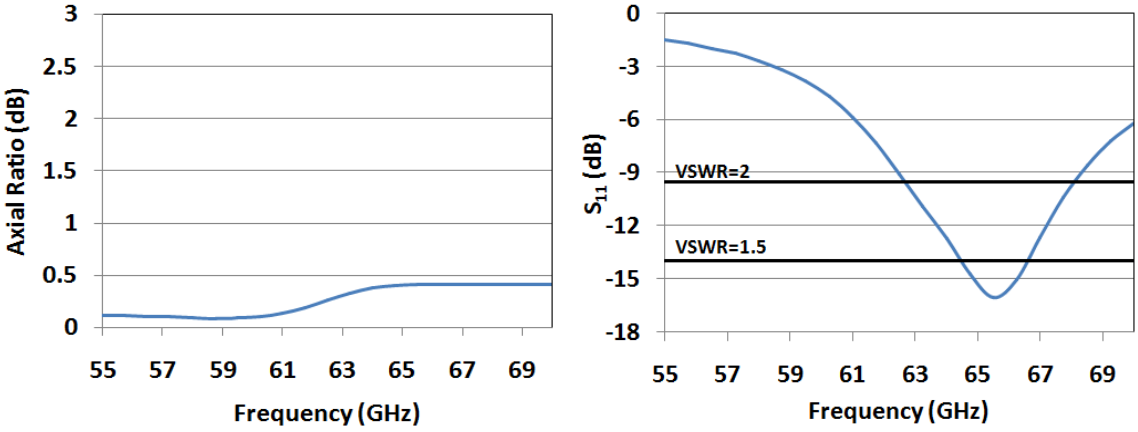


Figure 5: Return loss to determine the distance between two feed points *d*.



(a) Axial Ratio (b) Return Loss

Figure 6: Axial ratio and reflection.

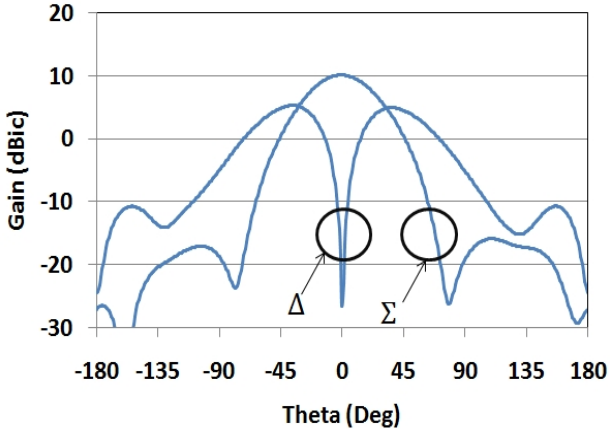


Figure 7: Radiation Pattern

References

[1] J. Hirokawa et al., "Millimeter-wave dipole antenna on a thick resin layer on the back side of a silicon CMOS chip", IEIEC Tech. Rep., AP2008-217, pp33-36, March 2009.

[2] M.S. Smith et al., "Analysis of radiation pattern effects in sequentially rotated arrays", Microwaves, Antenna and Propagation, IEE Proceedings, Vol. 141, No.4, pp.313-320, Aug 1994.